ExaNoDe

EUROPEAN EXASCALE PROCESSOR MEMORY NODE DESIGN

FLOPs will cost less than on-chip data movement.

The Cost of Data Movement in 2018

Wafer cost

ASP ↗ $19620
$9885 $11881 $14707
16nm 10nm 7nm 5nm

pico joules / bit
now · 2018

IC design cost

NRE ++ $1348M
$38M $67M $132M $273M $593M
28nm 20nm 16nm 10nm 7nm 5nm
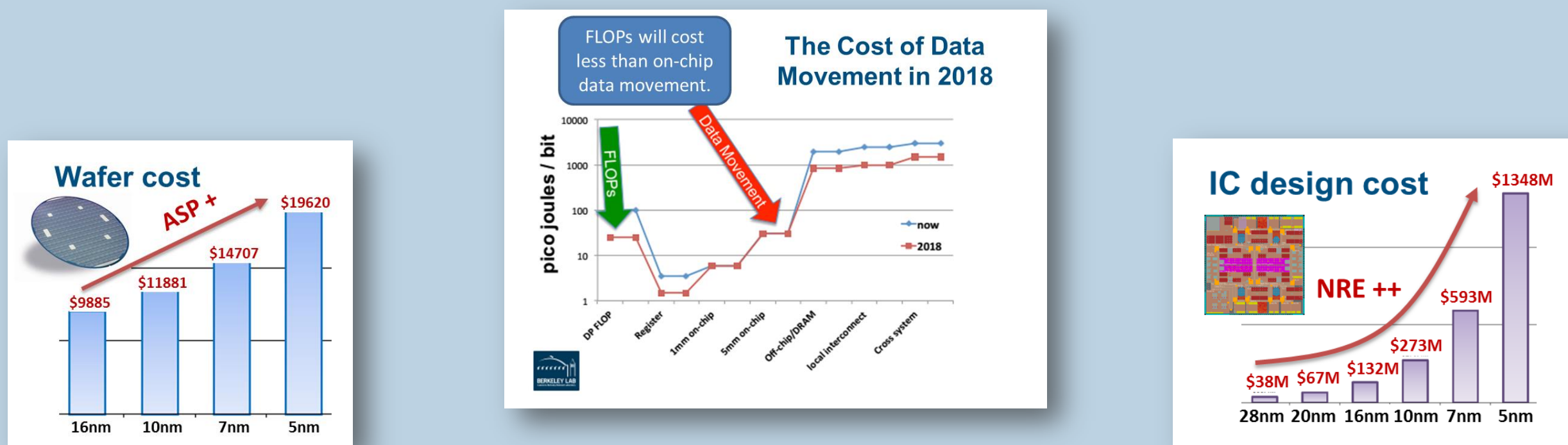
AFFORDABILITY
EVERYTHING CLOSE
POWER EFFICIENCY

INTEGRATION TECHNOLOGIES

- Chiplet on active interposer integration
- Multi-chip-Modules

Micro-bump — Chiplet
TSV — Interposer
Bump — Package substrate
Balls

Multi-chip-Module

VISION

CORE TECHNOLOGIES

Coordinator
CEA
ARM
Bull atos technologies
BSC Barcelona Supercomputing Center · Centro Nacional de Supercomputación
CNRS dépasser les frontières
ETH zürich
FORTH Institute of Computer Science
Fraunhofer
JÜLICH FORSCHUNGSZENTRUM
KALRAY
MANCHESTER 1824 The University of Manchester
scapos
Virtual Open Systems

ExaNoDe

web: www.exanode.eu

ARCHITECTURE

- ARMv8 processors
- Scale-out architecture

EURO SERVER

Coherent island: ARMv8-A Cores L1, L2, Coherent Interconnect	Coherent island: ARMv8-A Cores L1, L2, Coherent Interconnect	Coherent island: ARMv8-A Cores L1, L2, Coherent Interconnect	Coherent island: ARMv8-A Cores L1, L2, Coherent Interconnect

Multi-level Global Interconnect for coherent island communication

Local & Coherent Address Space	Local & Coherent Address Space	Local & Coherent Address Space	Local & Coherent Address Space

Shared I/O

Memory scheme principles: UNIMEM
1. *Each memory page can be cacheable to a single owner (coherent island) either locally or remotely but not both.*
2. *A processor (or DMA) can access any page in the system through the page owners coherent interconnect.*

Compute Node

Inter-device bridging

Compute Node example with 4 coherent islands

PROJECT OUTLINE

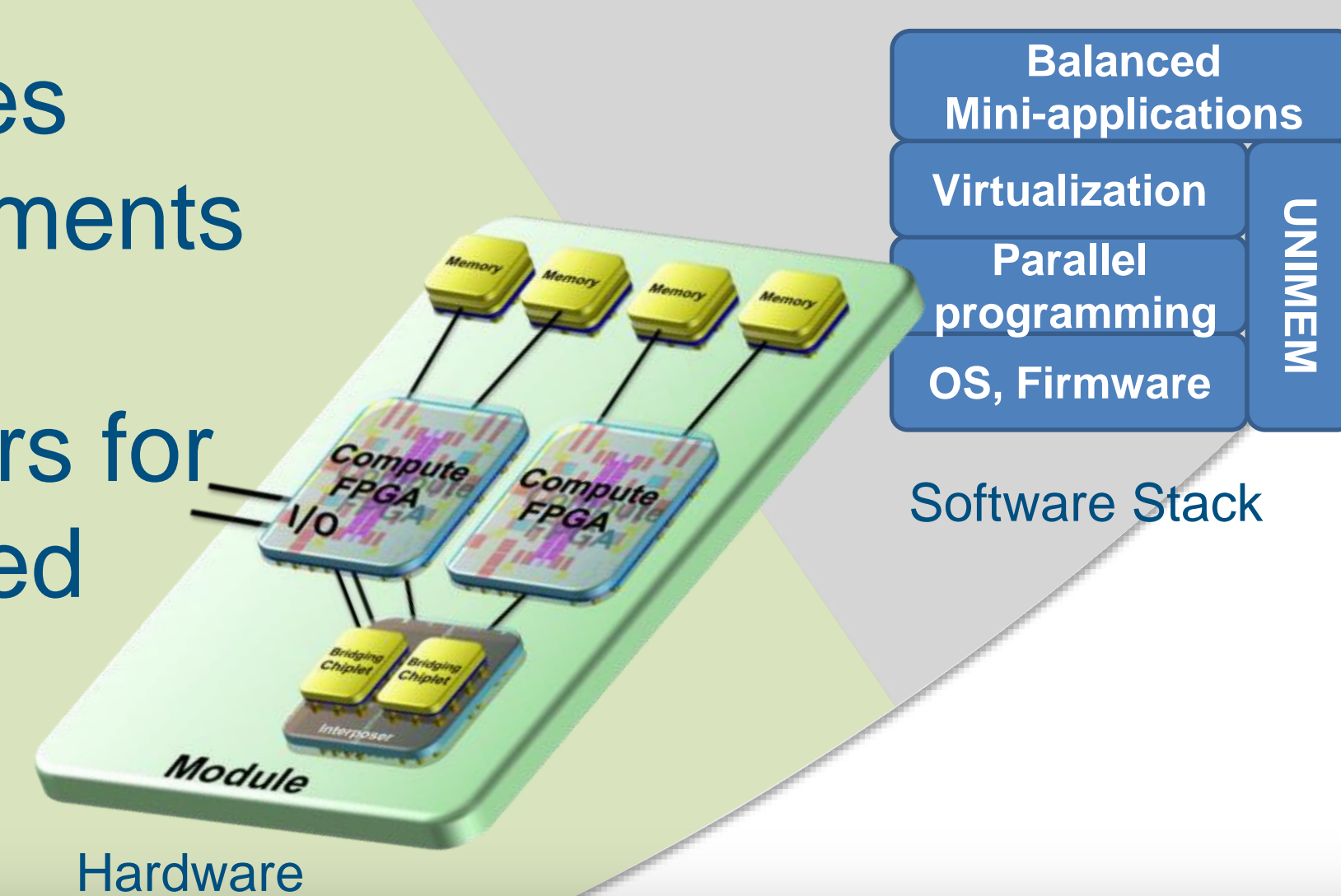| Project title	European Exascale Processor Memory Node Design
Start	October 1st, 2015
Duration	36 months
Call ID	H2020-FETHPC-2014
Topic	FETHPC-1-2014: HPC Core Technologies, Programming Environments and Algorithms for Extreme Parallelism and Extreme Data Applications
Budget	8.6 M€

OBJECTIVES

EXANODE PROOF-OF-CONCEPT (PoC)

- Deliver a compute node integrating core technologies consistent with the HPC system sizings and requirements for exascale computing.
- Validate the ExaNoDe core technologies as enablers for European exascale HPC in an appropriately balanced integrated PoC solution.
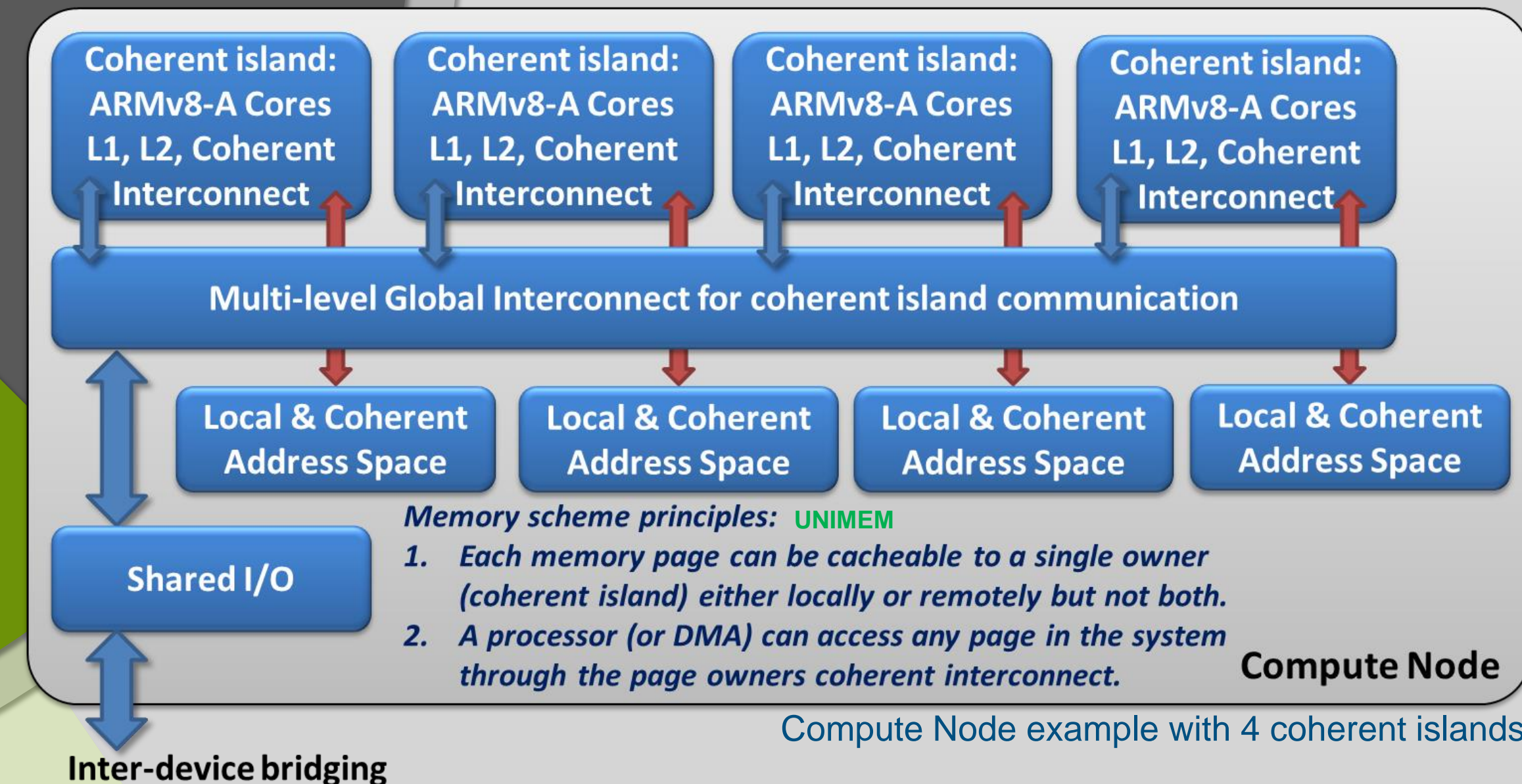
SOFTWARE STACK:
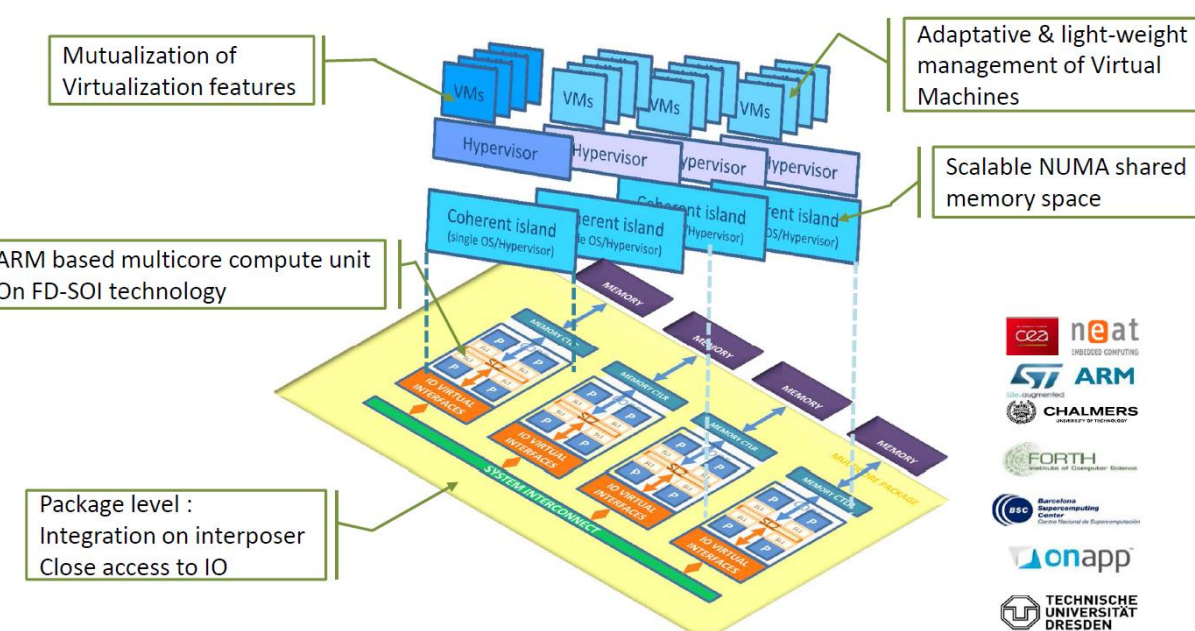
- UNIMEM memory scheme
- Virtualization

Balanced Mini-applications
Virtualization
Parallel programming
OS, Firmware
UNIMEM

Software Stack

Compute FPGA I/O
Compute FPGA

Module

Hardware

ExaNoDe as part of a global strategy

EURO SERVER

redesigns the entreprise server:

Lower cost through system integration
Energy efficiency : low-power 64 bit processor and more efficient software
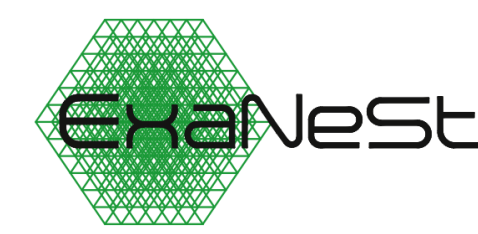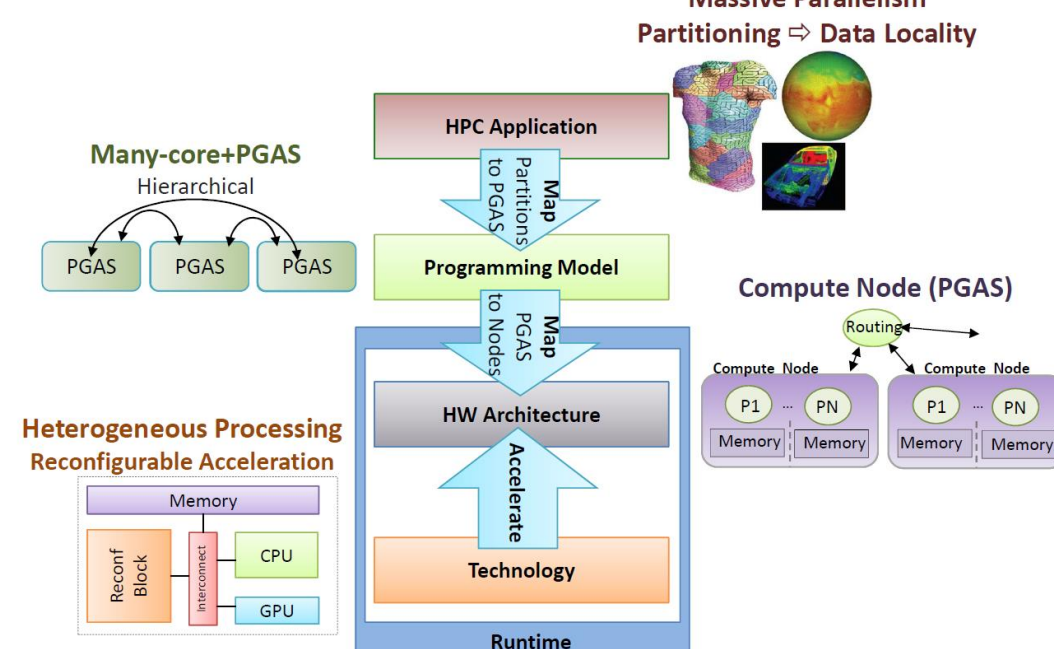**M**utualization (sharing) of I/O resources

Mutualization of Virtualization features
Adaptive & light-weight management of Virtual Machines
ARM based multicore compute unit On FD-SOI technology
Scalable NUMA shared memory space
Package level : Integration on interposer Close access to IO

www.euroserver-project.eu

ECOSCALE

Energy-Efficient Heterogeneous COmputing at exaSCALE

focuses on acceleration

Massive Parallelism Partitioning ⇒ Data Locality

Many-core+PGAS Hierarchical
HPC Application
PGAS · PGAS · PGAS
Programming Model
Compute Node (PGAS)
HW Architecture
Heterogeneous Processing Reconfigurable Acceleration
Technology
Runtime

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EXANEST
Storage, Interconnect, Cooling

European Exascale System Interconnect and Storage

Storage: fast, distributed in-node non-volatile memory
Interconnect: low-latency, unified compute & storage traffic
Packaging: advanced, liquid-cooled
App's: real, scientific and datacenter
Prototype: 1000+ ARM cores
from *EuroServer*: ARM nodes with UNIMEM address space & shared I/O
from *ExaNoDe*: Chiplets, Si Interposer
with *ECOSCALE*: Heterogeneous. ARM+FPGA's

Iceotope Ltd: *Fully Immersed Cooling Technology*

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