Welcome!

European Exascale Processor & Memory Node Design

This project has received funding from the European Union's Horizon 2020 research and innovation programme under grant agreement No 671578

ExaNoDe

- ExaNoDe develops key technologies for compute nodes leading towards a future Exascale capability comprising:

System Architecture	Silicon Integration	Software

• ARMv8
• Coherent island
• Global Address Space
	• 3D Integration:
	  • Chiplet
	  • Active Interposer
	• Multi-Chip-Module:
	  • FPGA, Memory
		• FW, OS
		• Virtualization
		• Programming models
		• Runtimes
		• Mini-apps

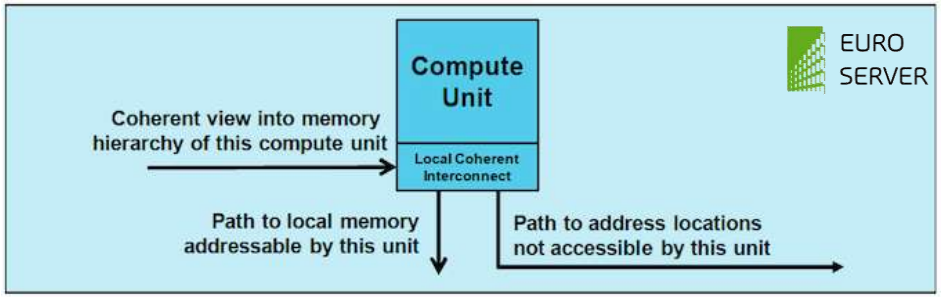
👍 Energy efficiency 👍 Scalability	👍 Design/manufacturing costs 👍 Heterogeneity & Specialization	👍 Scalability 👍 Co-design

- All combined in an integrated prototype.

ExaNoDe architectural approach

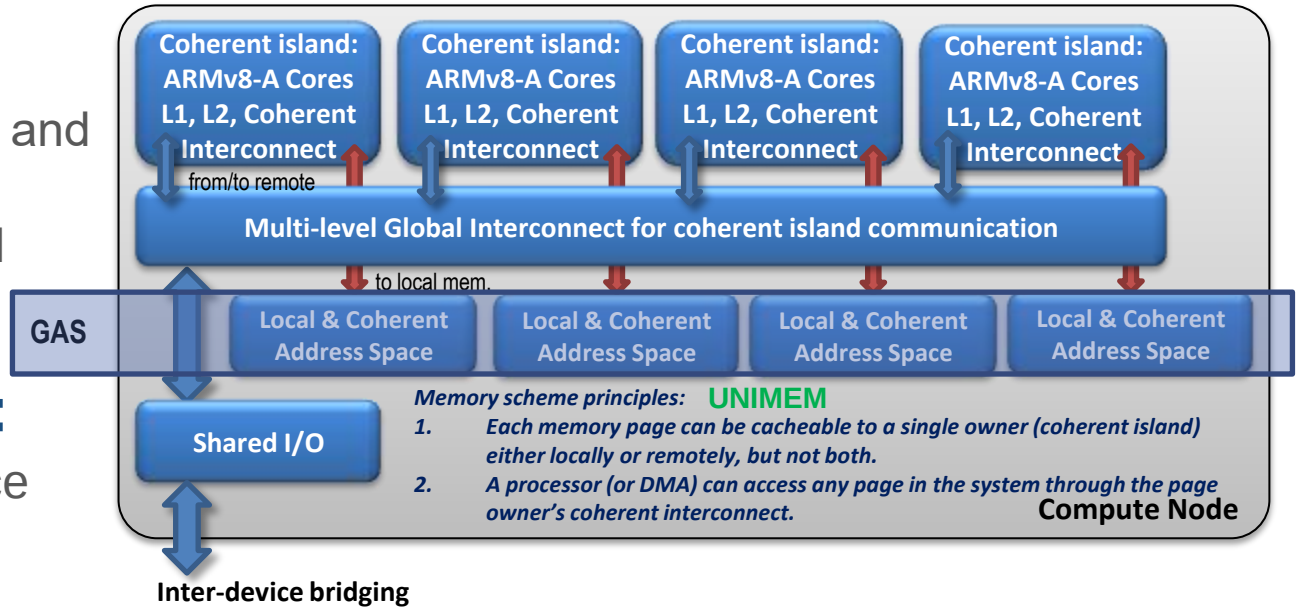
- **Coherent Island:**
  - Many ARMv8 processors
  - Local coherent interconnect
  - Path to local memory
  - Path “to remote” memory locations
  - Path “from remote” compute units

Source: John Goodacre – DATE’13



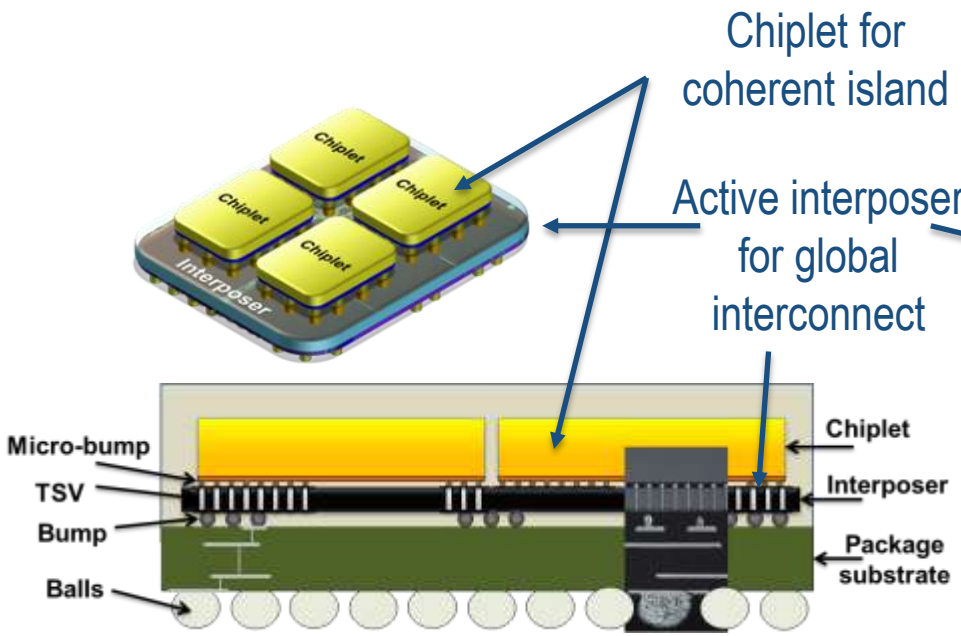
- **Compute Node:**
  - Scale-out with “from” and “to” remote port connections to global network

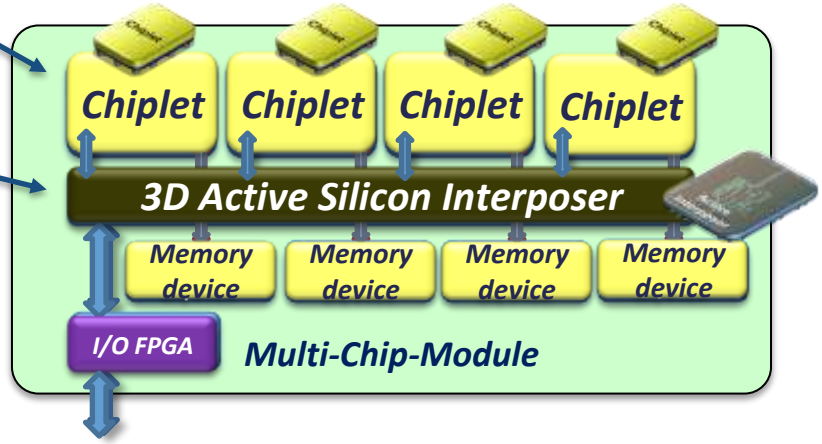
- **Memory scheme:**
  - Global Address Space with UNIMEM



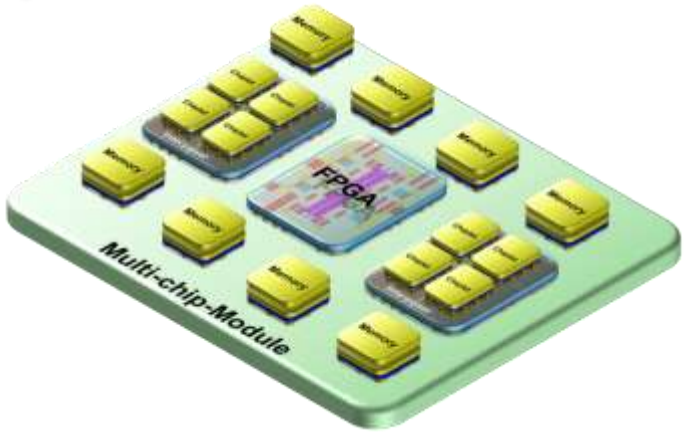
ExaNoDe integration approach

- **3D integration with an active silicon interposer and chiplets:**



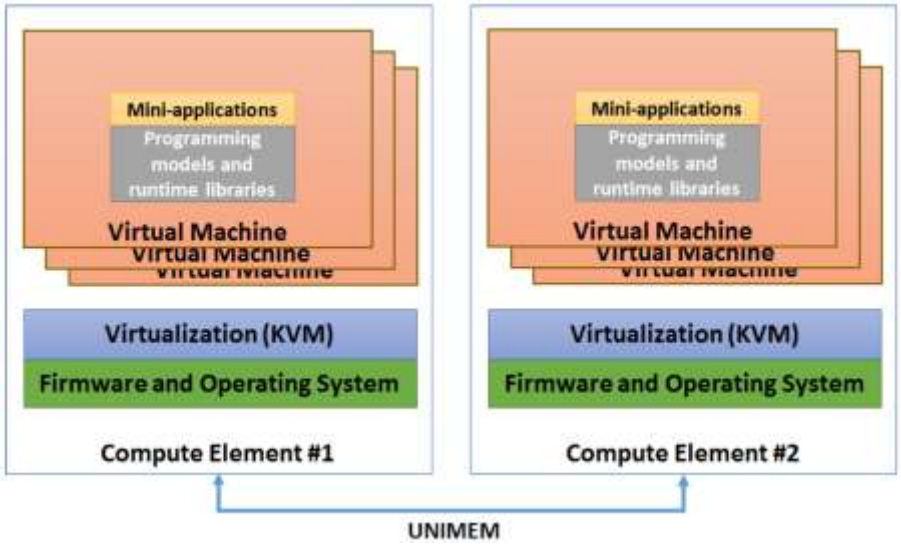


- **Multi-chip-Module integration for bare dies**



ExaNoDe SW

- **Mini-apps for co-design:**
  - Select HPC applications that will be used to co-design the ExaNoDe architecture.
- **Software infrastructure:**
  - Deploy a software ecosystem for the ARM-based Compute Node in conjunction with the UNIMEM system architecture.
- **Evaluation:**
  - Analyse and compare the ExaNoDe architecture.

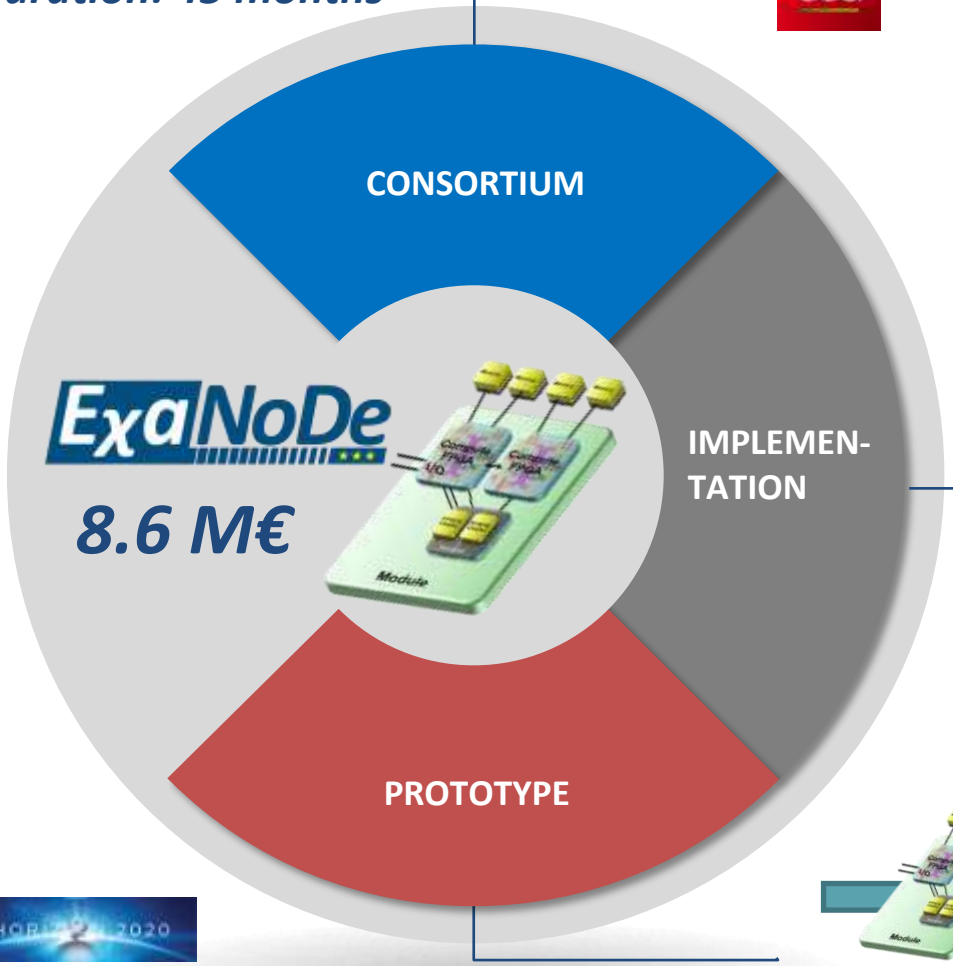


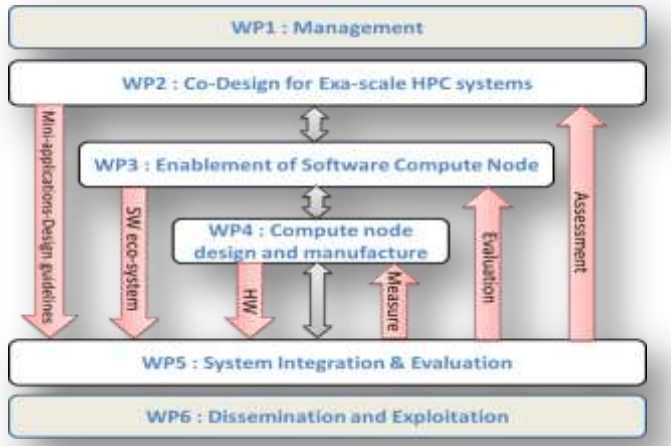
ExaNoDe Software Architecture

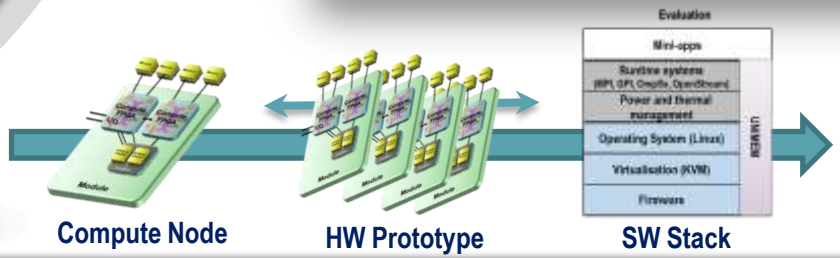
Project Implementation

Start: October 1st, 2015
Duration: 45 months

Coordinator







ExaNoDe Prototype: Technologies

ExaNoDe core technologies portfolio

Compute element & Accelerators
Low Power Processors
CNN accelerator
FPGA
Thermal and Power Management

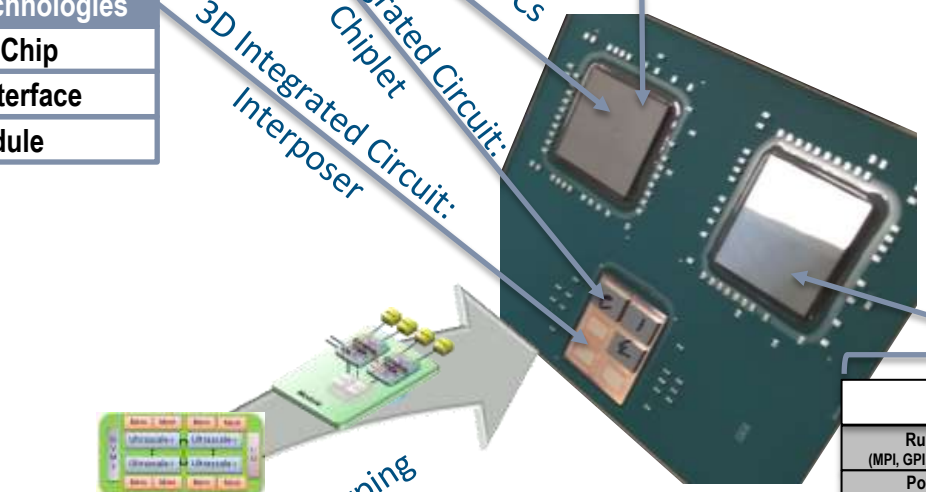
Integration & Nanotechnologies
3D Network-On-Chip
Enhanced 2.5D interface
Multi-Chip-Module

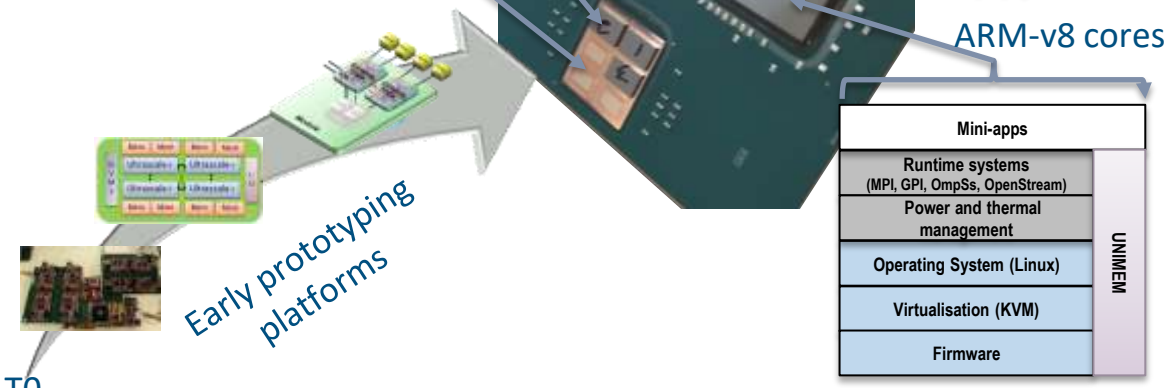
UNIMEM
Atomic Service
Packetizer and Virtualized MBOX

Virtualization techniques
Checkpointing
UNIMEM

Programing models
PGAS, GPI-2
MPI
OmpSs
OpenStream

Mini-apps
BQCD
HydroC
KKRnano
MiniFE



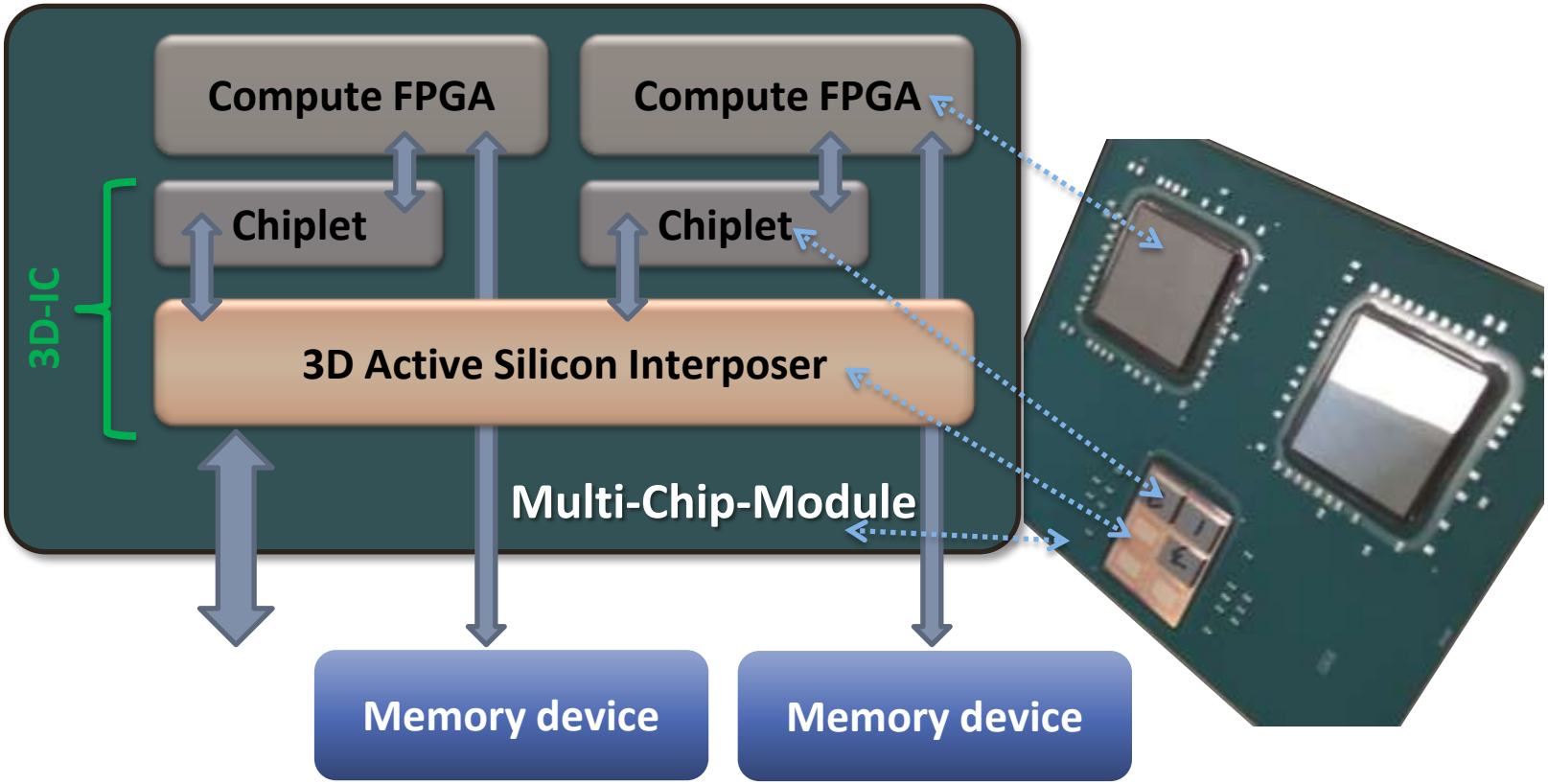


Early prototyping platforms

T0

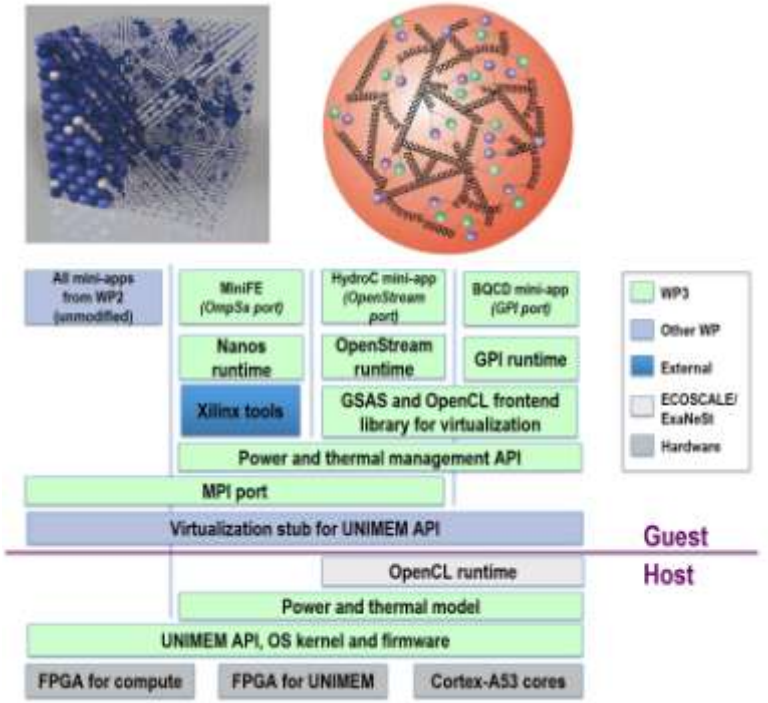
Multi-Chip-Module Prototype

ExaNoDe Prototype: Multi-Chip-Module



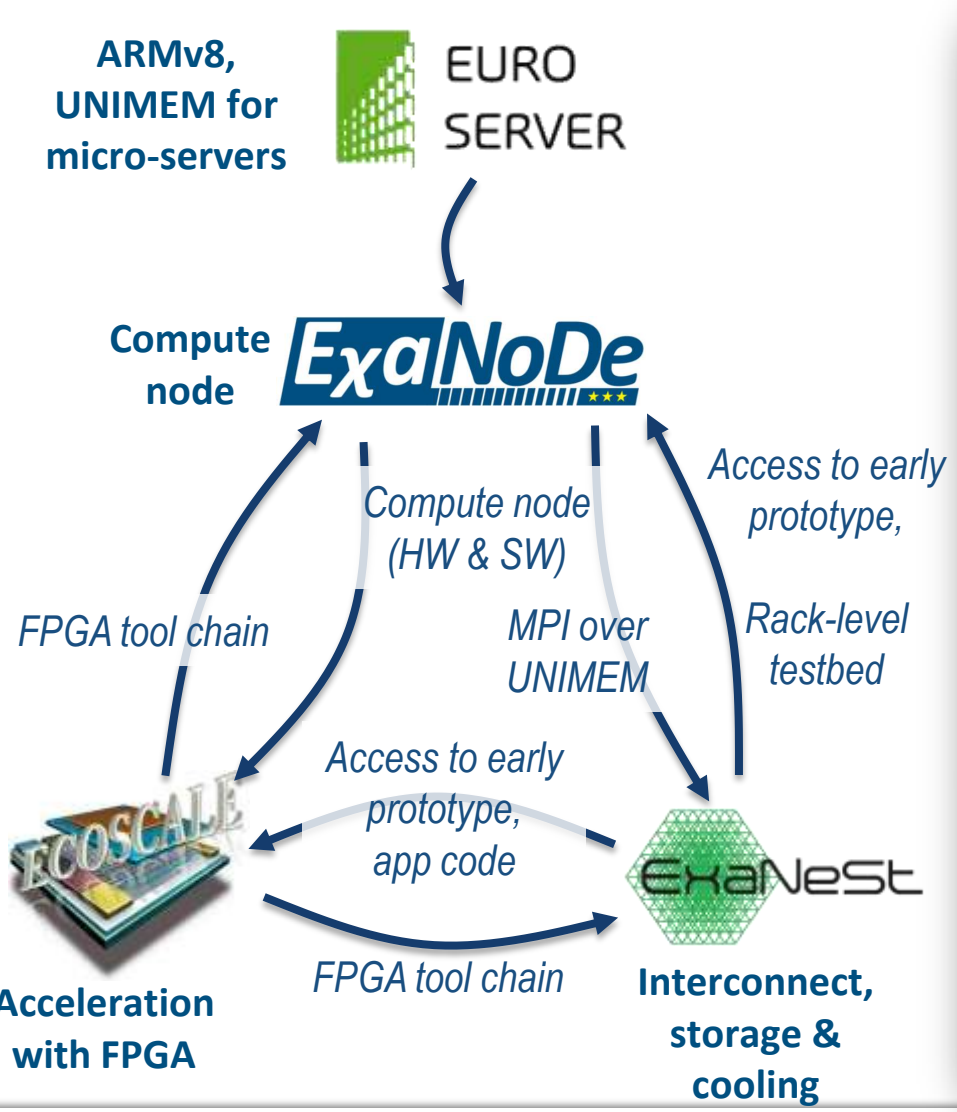
ExaNoDe Prototype: Daughter Board

- **ExaNoDe SW stack**



- **ExaNoDe board with Multi-Chip-Modules, 3D Integrated Circuit and FPGA bare dies**

Eco-system



ExaNoDe as part of a global strategy

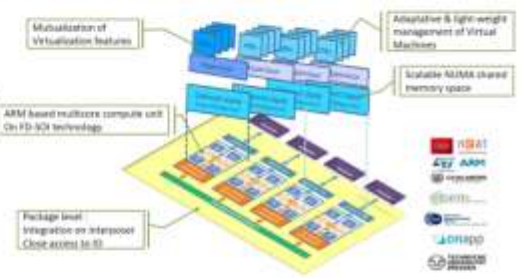
EURO SERVER

redesigns the entreprise server:

Lower cost through system integration

Energy efficiency : low-power 64 bit processor and more efficient software

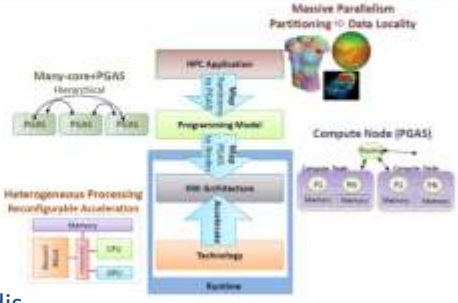
Mutualization of I/O resources



Source: Isabelle Dor

ECOSCALE

focuses on acceleration



Source: Iakovos Mavroidis

European Exascale System Interconnect and Storage - www.exanest.eu

ExaNeSt

Storage, Interconnect, Cooling

Storage: fast, distributed in-node non-volatile memory
Interconnect: low-latency, unified compute & storage traffic
Packaging: advanced, liquid-cooled
App's: real, scientific and datacenter
Prototype: 1000+ ARM cores
from *EuroServer*: ARM nodes with UNIMEM address space & shared I/O
from *ExaNoDe*: Chiplets, Si Interposer
with *ECOSCALE*: Heterog. ARM+FPGA's

Icetope Ltd: *Fully Immersed Cooling Technology*

Source: Manolis Marazakis

Thank you!

European Exascale Processor & Memory Node Design

www.exanode.eu