Welcome!

European Exascale Processor & Memory Node Design

This project has received funding from the European Union's Horizon 2020 research and innovation programme under grant agreement No 671578

Silicon interposer integration combined with novel system architecture for energy-efficient and heterogeneous compute node: the ExaNoDe solution

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CEA-LETI
June 28th 2018

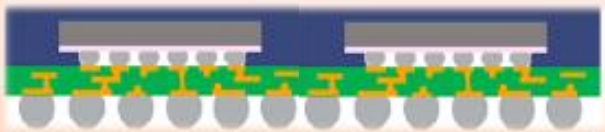
Post Moore Interconnects Workshop
ISC High Performance 2018
Frankfurt, Germany

Advanced Packaging Integration: Technologies

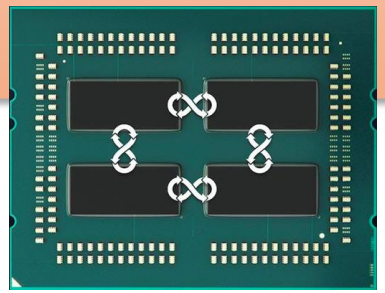
Advanced Packaging Integration

SiP

Multi-Chip-Module



Interconnect density: 100µm x 100µm

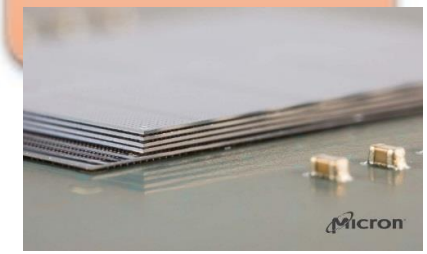


Source: AMD EPYC 7260, 4-chiplet chip

3D

Die stacking

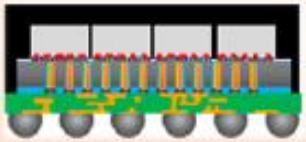
Interconnect density: 10µm x 10µm



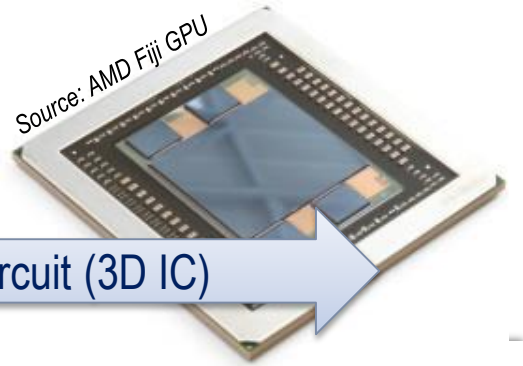
Source: Micron High-Bandwidth-Memory

2.5D

Interposer based



Interconnect density: 10µm x 10µm

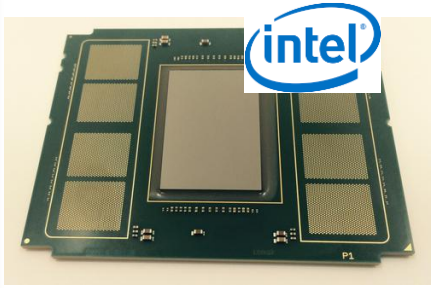


System-in-Package

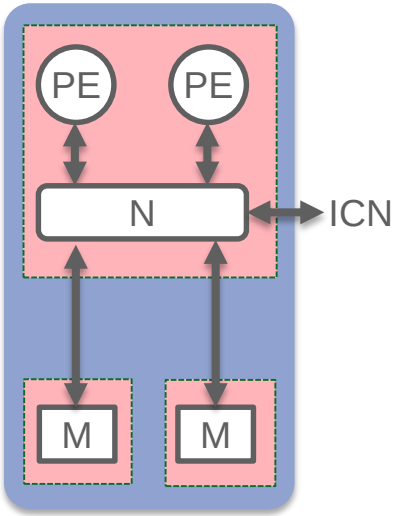
3D Integrated-Circuit (3D IC)

Advanced Packaging Technologies for HPC

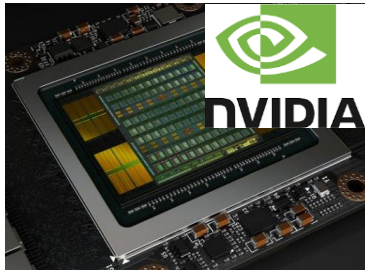
PROCESSOR



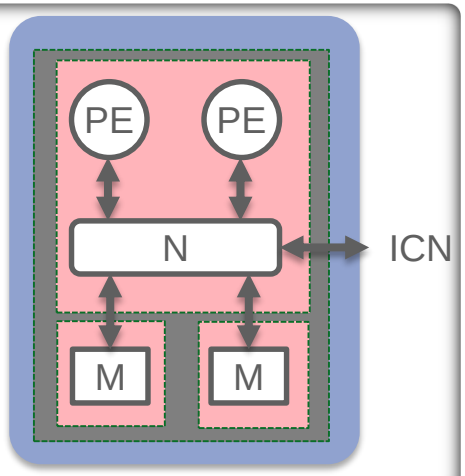
Multi-Chip-Module



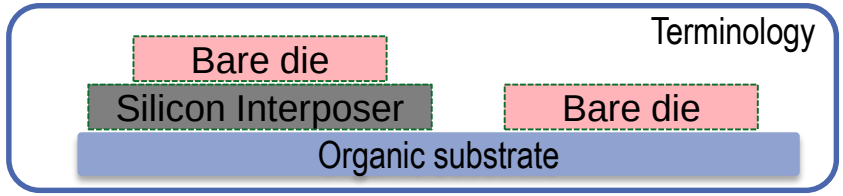
ACCELERATOR



Interposer based Integration

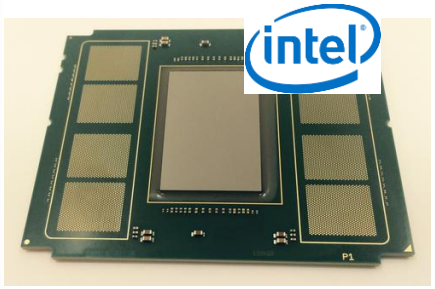


- **Benefits of advanced packaging for HPC:**
  - **Performance scaling** for processor: one or two die per socket,
  - **Memory bandwidth** for accelerator: interposer integration of High Bandwidth Memories.
- **Limitation:**
  - **Lack of modularity for heterogeneous systems**: coarse grain heterogeneous integration resulting in high power consumption between compute elements.

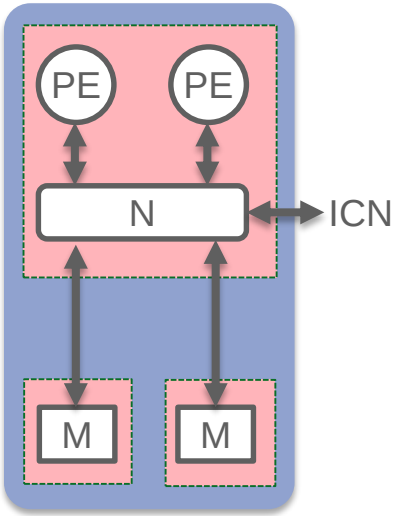


The ExaNoDe solutions for Heterogeneous and Modular Computing

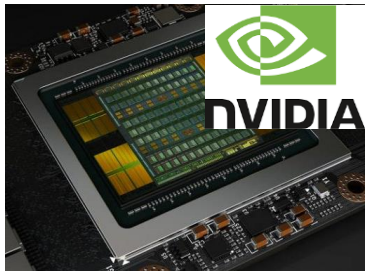
PROCESSOR



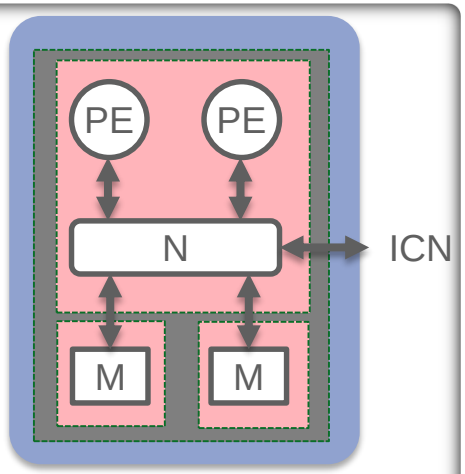
Multi-Chip-Module



ACCELERATOR



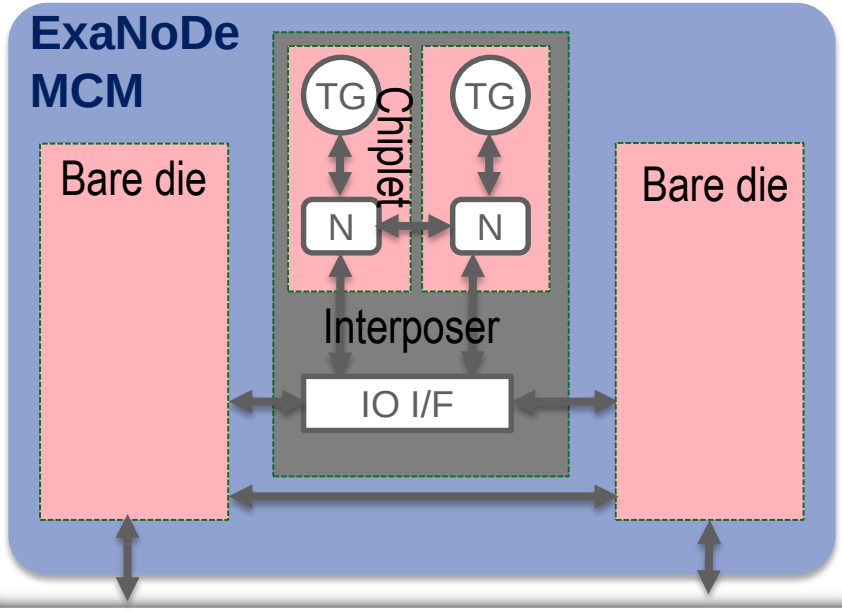
Interposer based Integration



HETEROGENEOUS AND MODULAR COMPUTING

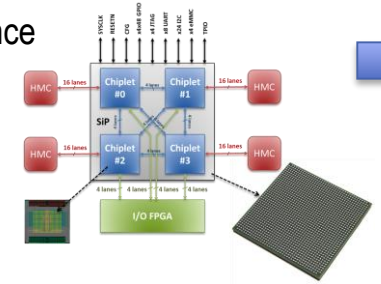
ExaNoDe

- ***Chiplet* for modularity,**
- ***Silicon Interposer* for low power die-to-die communication and I/O interface,**
- ***Multi-Chip-Module* for reconfigurable accelerators (FPGA).**



Advanced Packaging among European HPC Projects

MCM reference design

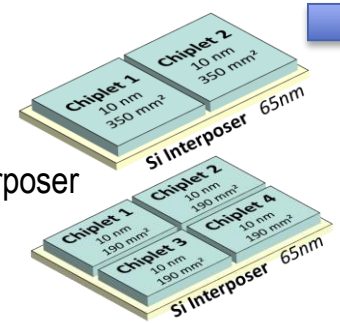


EURO SERVER

MICRO-SERVER

Chiplet approach
Multi-Chip-Module

Combined architecture / silicon interposer exploration

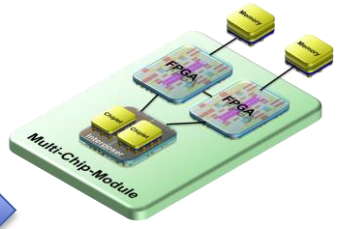


MONT BLANC

HPC

Silicon Interposer

Integrated prototype



HPC

Multi-Chip-Module

Silicon Interposer

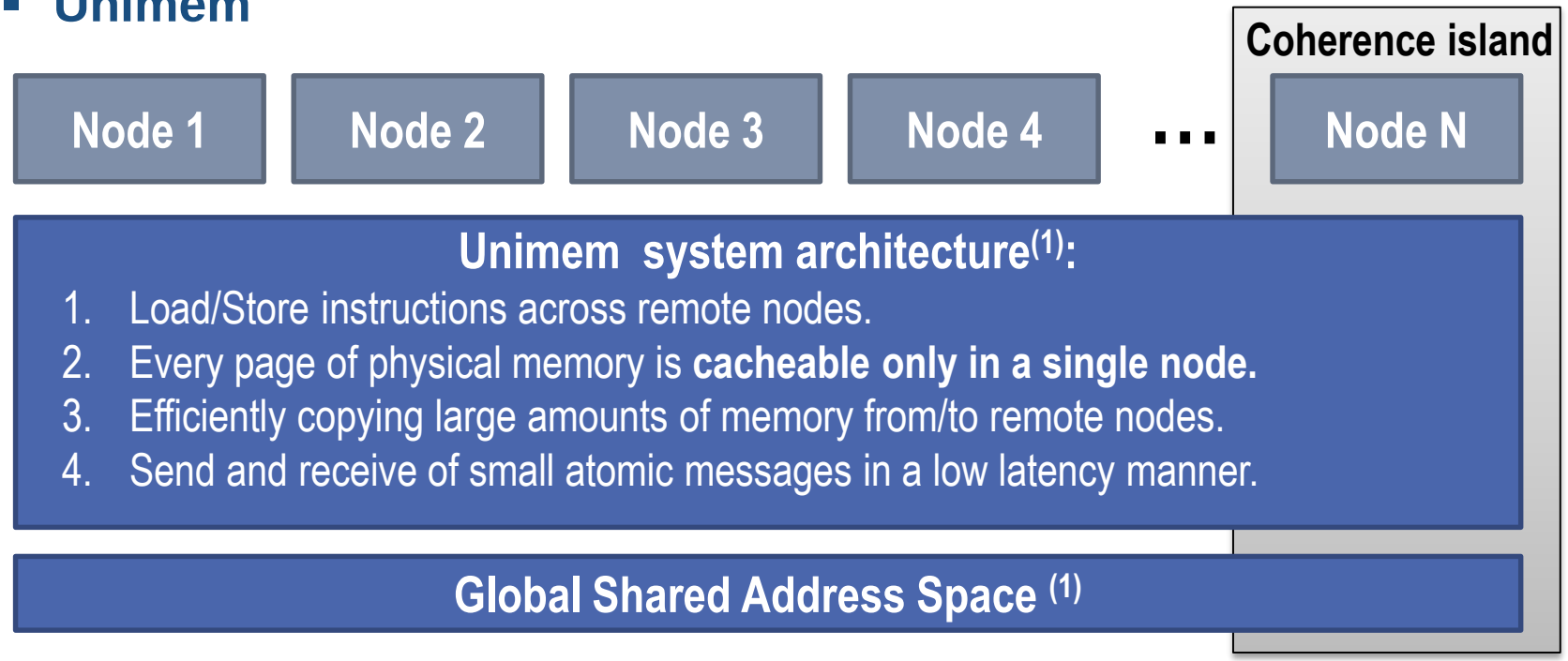
ExaNoDe

Advanced packaging ready for next generation HPC systems

2011-2016 | 2015-2018 | 2018…

ExaNoDe System Architecture

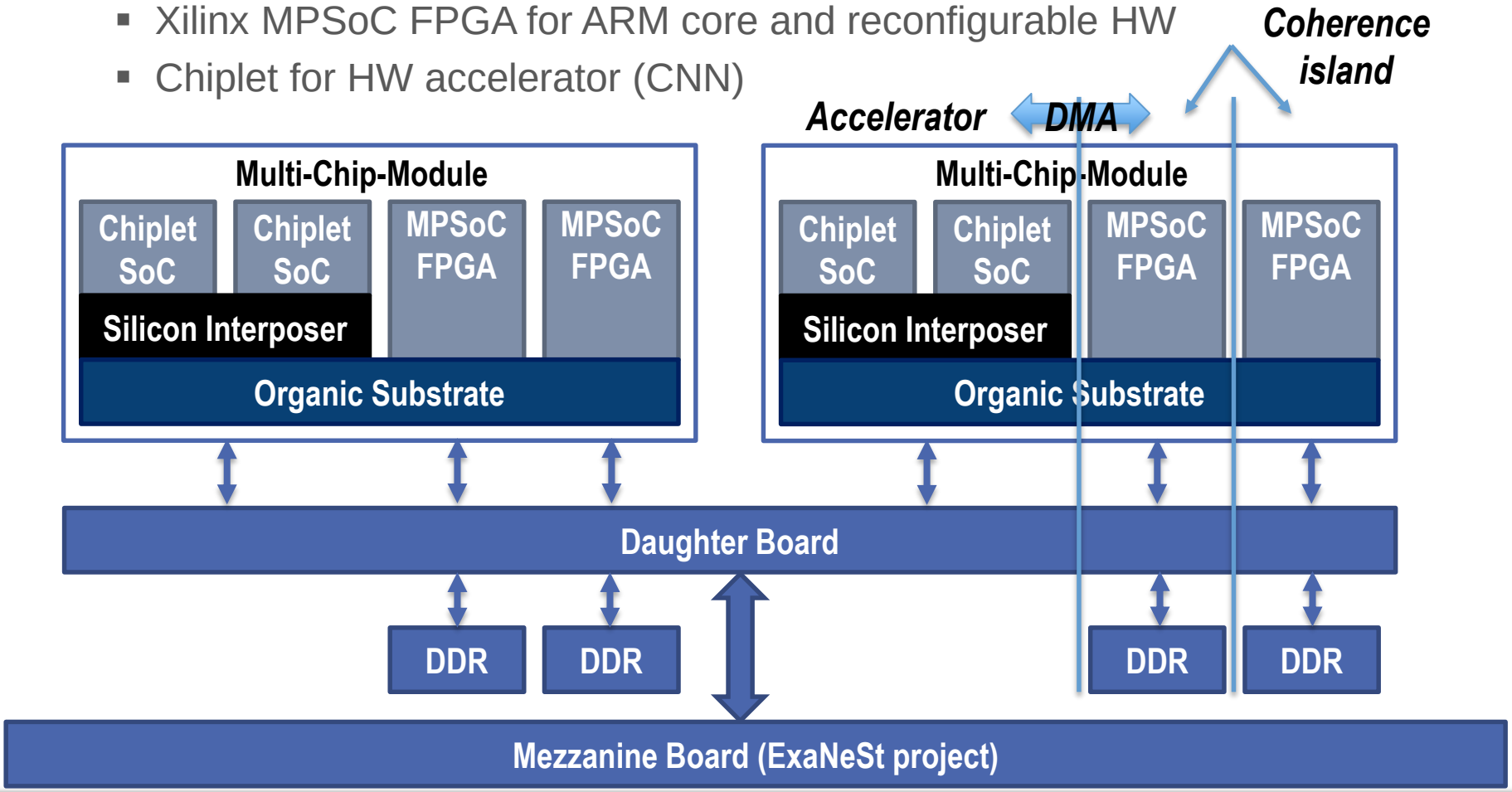
- **Node: 64-bit ARM core + HW accelerator + reconfigurable HW**
- **Global Shared Address Space**
- **Unimem**



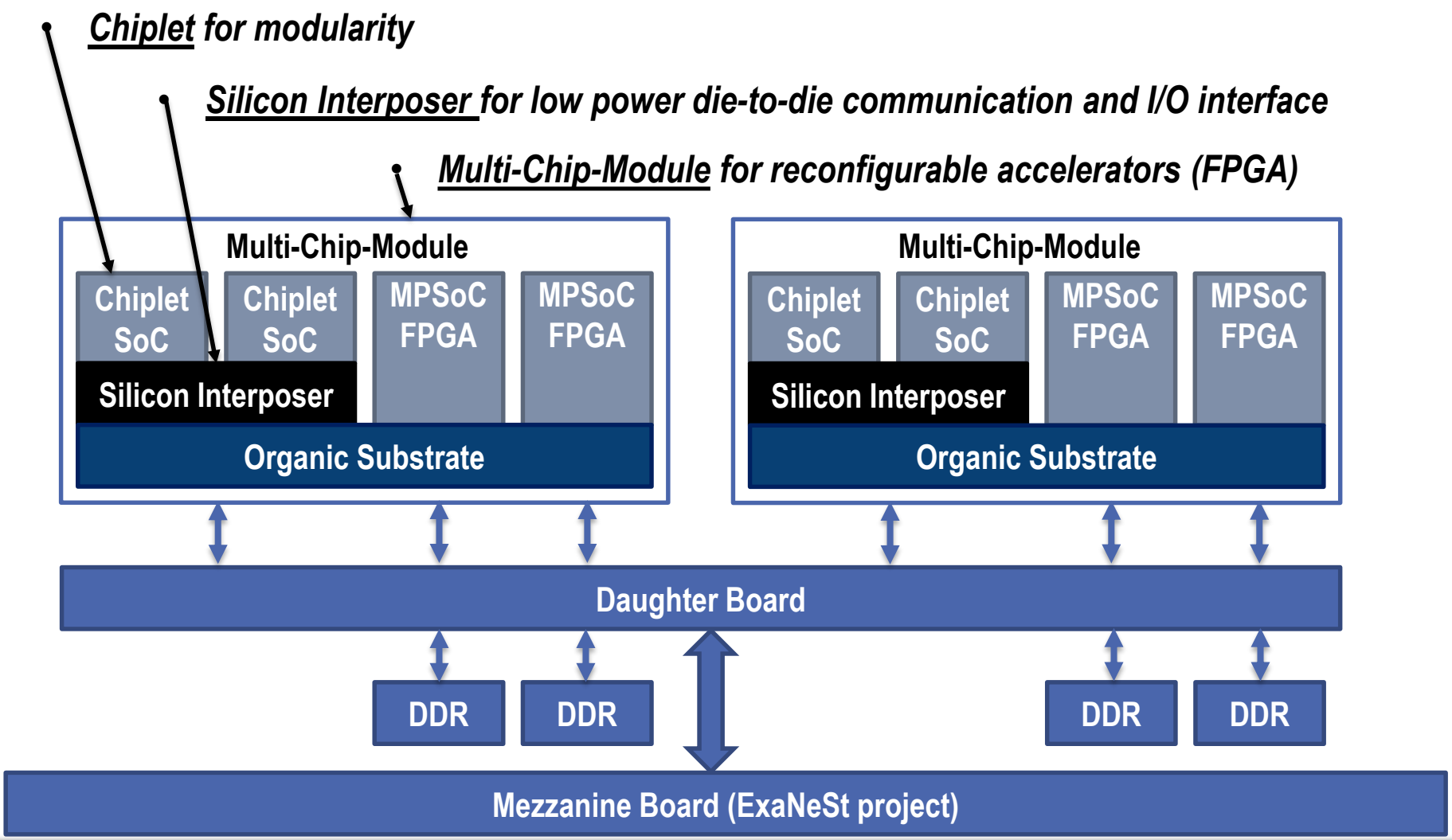
(1) source: **A Flexible & Efficient Shared Memory Abstraction with Minimal HW Assistance**; *Nikolaos D. Kallimanis - FORTH-ICS;* EuroEXA, ExaNeSt, ExaNoDe and EcoScale workshop, European HPC Summit Week 2018, Ljubljana, Slovenia

ExaNoDe HW Prototype: Integration Hierarchy

- **Node:**
  - Xilinx MPSoC FPGA for ARM core and reconfigurable HW
  - Chiplet for HW accelerator (CNN)

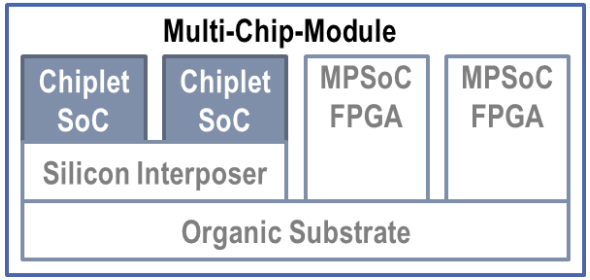


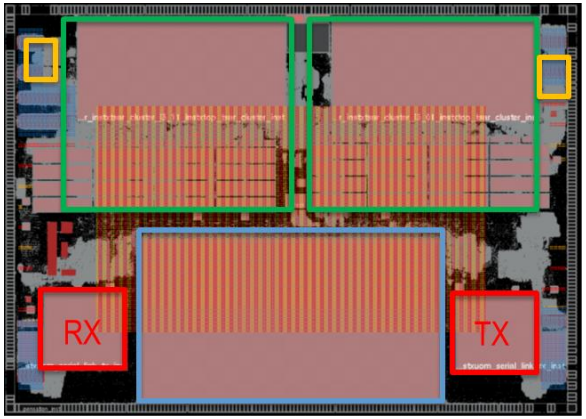
ExaNoDe HW Prototype: Integration Technologies

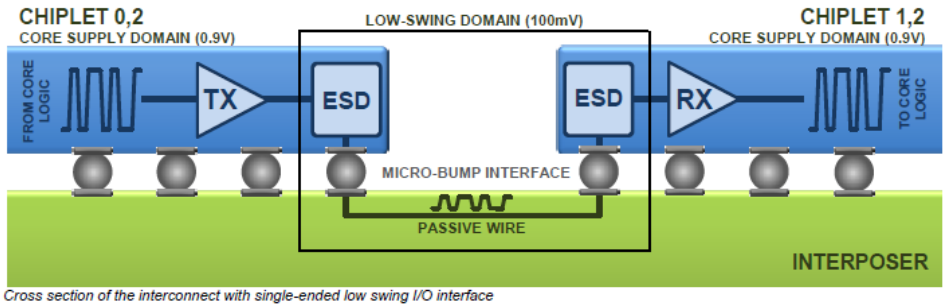


ExaNoDe HW Prototype: Chiplet

- **Objectives & Challenges:**
  - Modularity and low cost for fine grain heterogeneous integration
  - Ultra-low power communication between dies with fine pitch integration on interposer





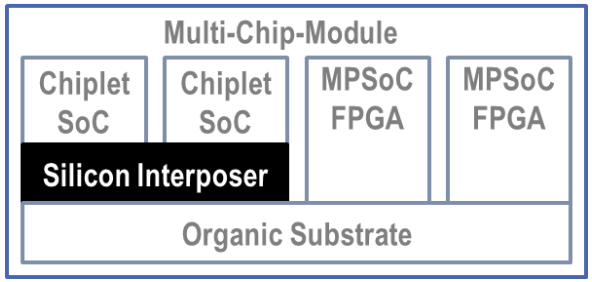


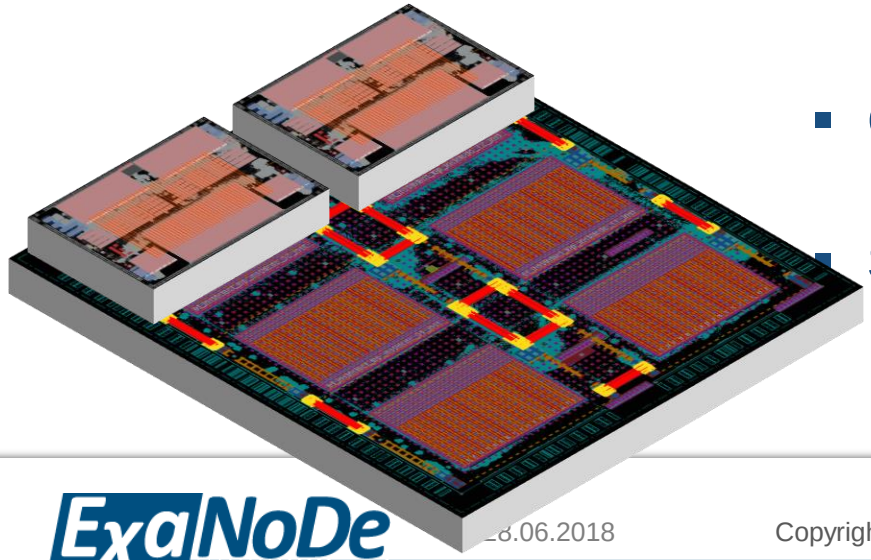
Cross section of the interconnect with single-ended low swing I/O interface

- **Architecture:**
  - Ultra Short Reach chiplet to chiplet fast link (UOM)
  - 3D Network-on-Chip interconnect with Interposer (CEA)
  - Convolutional Neural Networks (ETHZ)
  - Programmable Traffic generator (CEA)
- **28FDSOI STM process**
- **Micro-bumps:**
  - Ø 10 µm, pitch 20 µm
- **Status end of June 2018:**
  - wafers back from fab (including 3D steps) and ready for test and assembly

Silicon Interposer

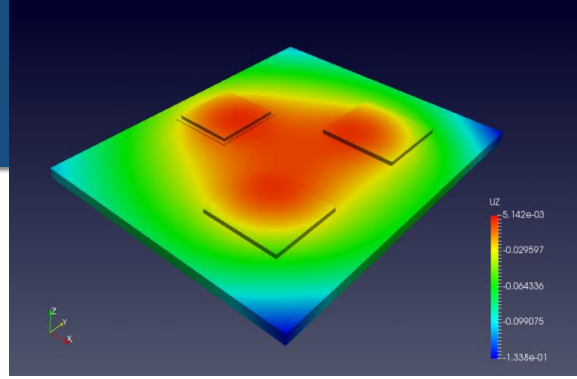
- **Reuse from INTACT project funded by the French ANR IRT Nanoelec program: "active interposer demonstrator"**
- **Objective & challenge:**
  - Low power and high bandwidth communications
  - Mix TSVs with logic



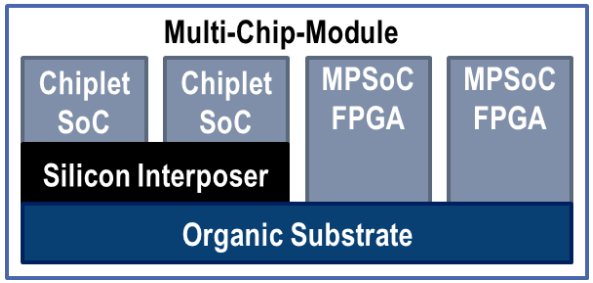


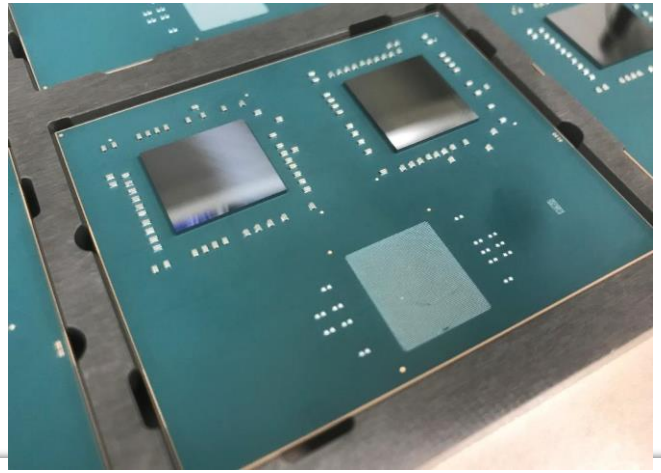
- **Architecture:**
  - FPGA interface
  - 3D Network-on-Chip interconnect with chiplet
  - Chiplet to chiplet interconnect with metal layers
  - Embedded DC-DC on the interposer for chiplet supply voltage
- **CMOS65 STM process, TSV middle**
  (Ø 10µm, Height 100µm)
- **Status end of June 2018:**
  - wafers back from fab (including 3D steps) and ready for test and assembly

Multi-Chip-Module (1/2)

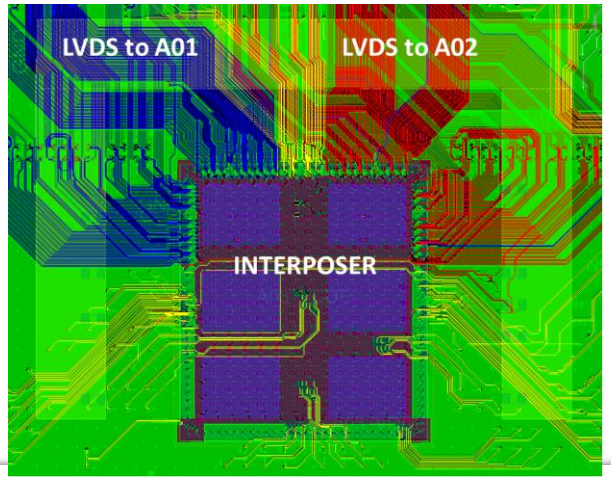


- **Objective & Challenge:**
  - Coarse grain heterogeneous integration
  - Warpage





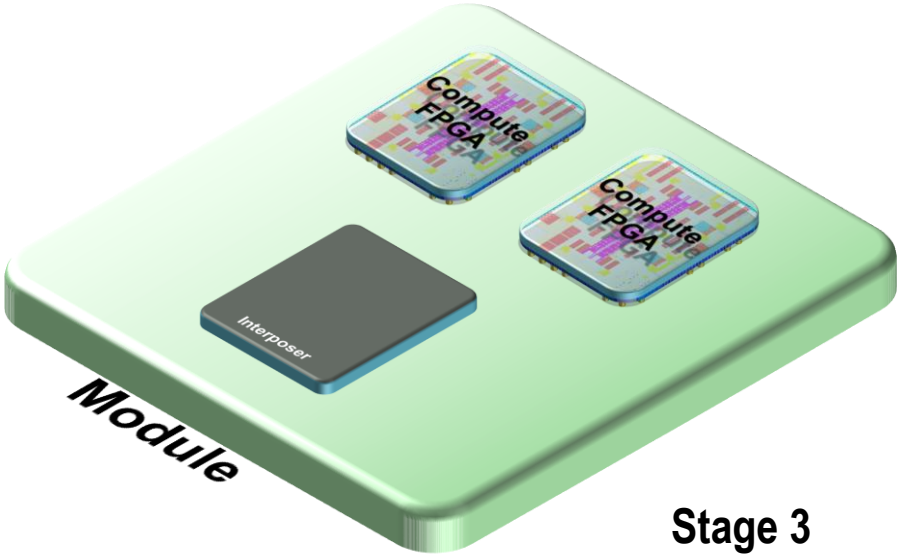
- **Architecture:**
  - Laminate substrate
  - Two FPGA bare dies and one silicon interposer
  - Cu/Ni lid
- **Design:**
  - Interposer routing to FPGA and decoupling capacitors:



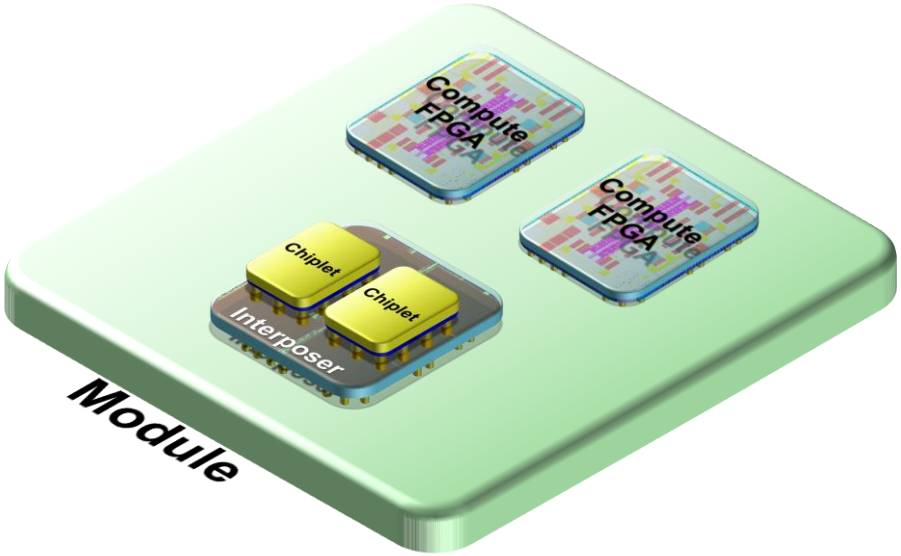
Multi-Chip-Module 2/2

- **Assembly process:**

Stage 1
- Decoupling capacitors, FPGAs and interposer placement (pick & place, flip chip)
- Mass reflow



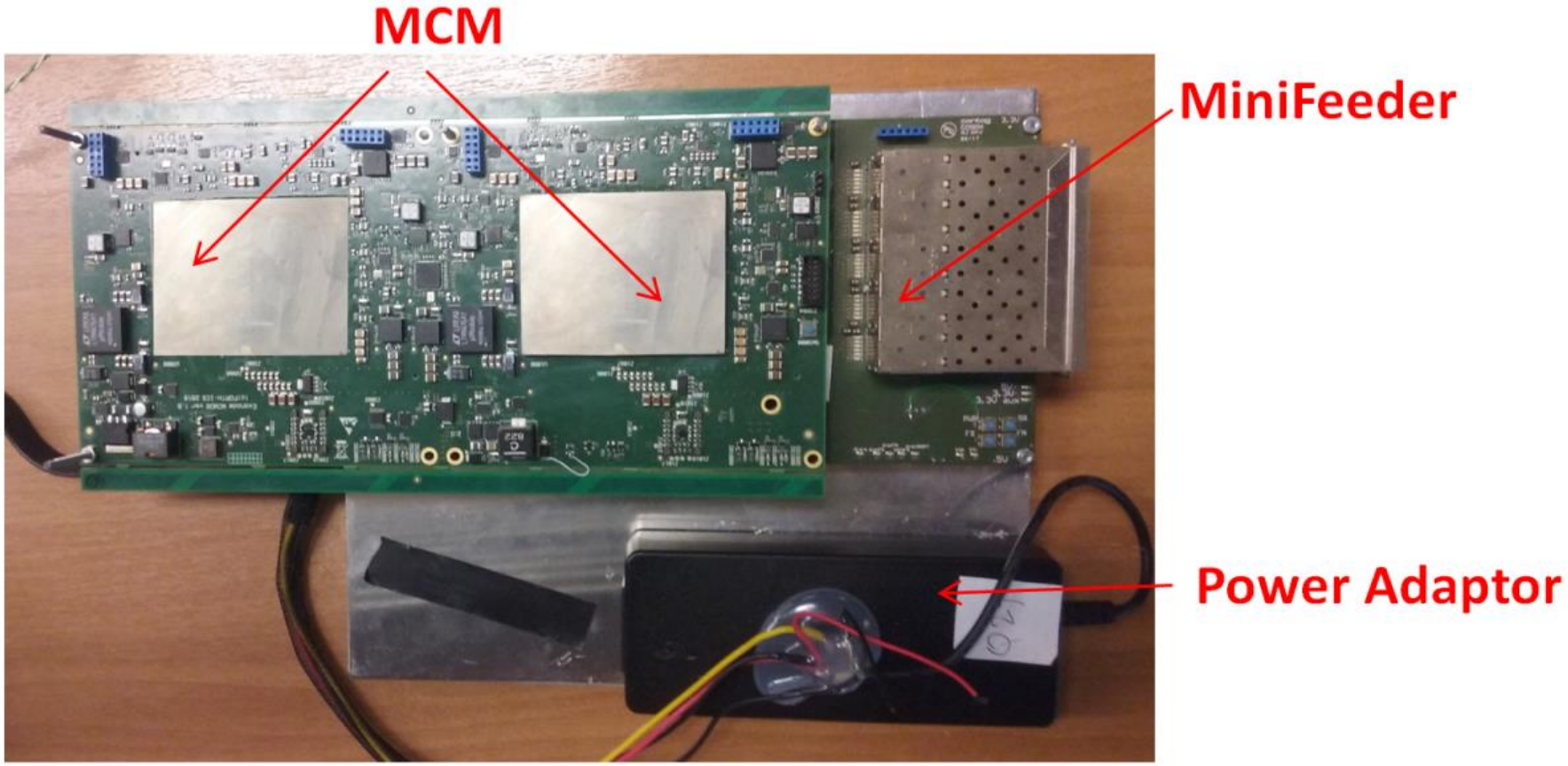
Stage 2
- Chiplets stacking on interposer by thermocompression bonding



Stage 3
- Copper lid placement
- BGA placement and reflow

ExaNoDe HW Prototype: Daughter Board

- **Objectives:**
  - To deploy ExaNoDe system prototype (HW + SW) in an HPC system environment compatible with ExaNeSt



Conclusion

- **Silicon Interposer integration:**
  - a key enabling technology for high performance and power efficient processors and accelerators.
- **ExaNoDe main innovations related to silicon interposer:**
  - 3D Integrated Circuit design solutions,
  - Ultra Short Reach chiplet-to-chiplet fast link,
  - 3D plug for chiplet-to-interposer data link,
  - Chiplet-on-Interposer-on-MCM assembly process.
- **ExaNoDe silicon interposer enables:**
  - Modularity thanks to chiplet design solutions,
  - Multi level of integration (Chiplet-on-Interposer-on-MCM) for power efficient heterogeneity.

Acknowledgements:

This project has received funding from the European Union's Horizon 2020 research and innovation programme under grant agreement No 671578

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Thank you!

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