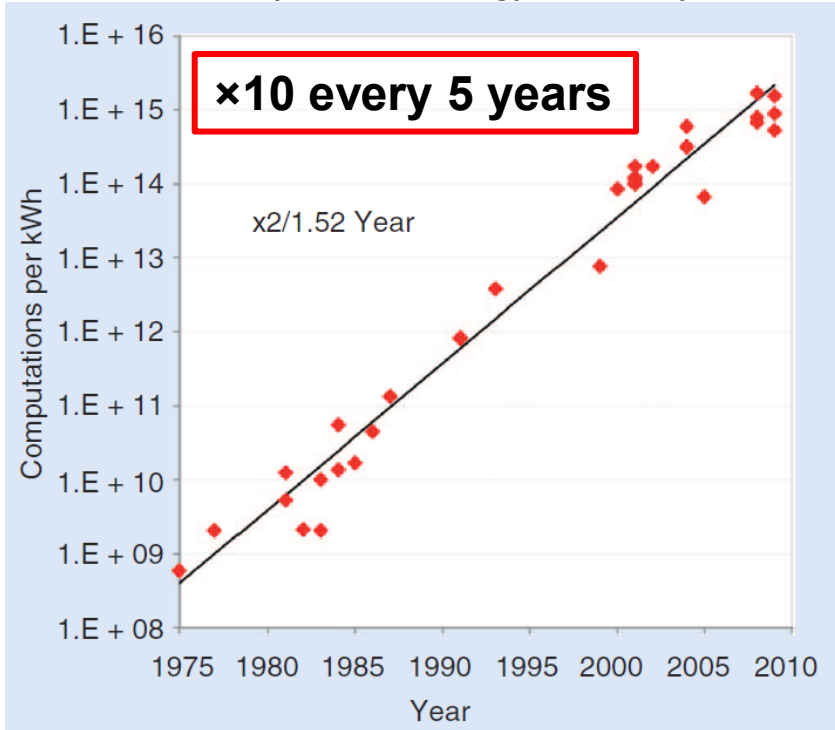


Ultra-Low Swing Transceiver for Energy Efficient Communication in 2.5-D Integrated Systems

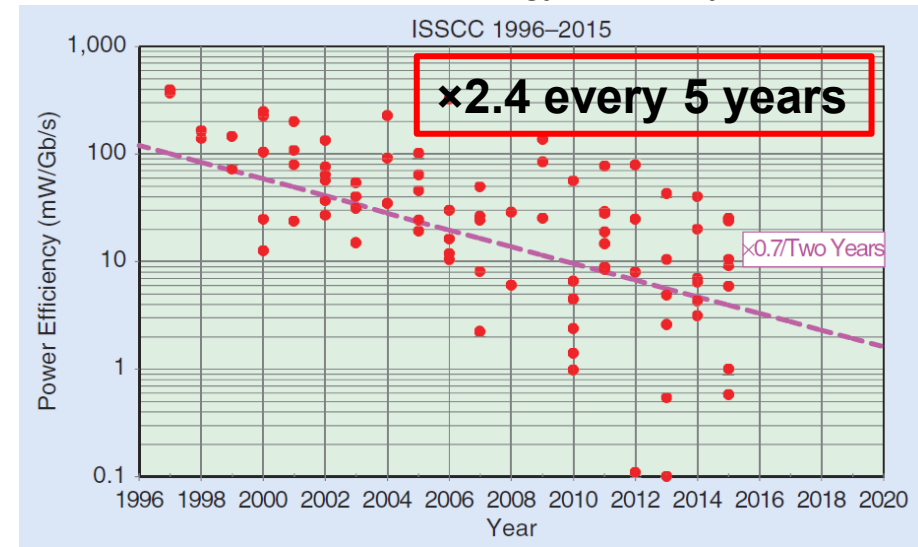
Przemyslaw Mroszczyk & Vasilis Pavlidis
School of Computer Science
The University of Manchester
M13 9PL, Manchester, UK

Why Communication matters?

Computation energy efficiency trend ¹⁾

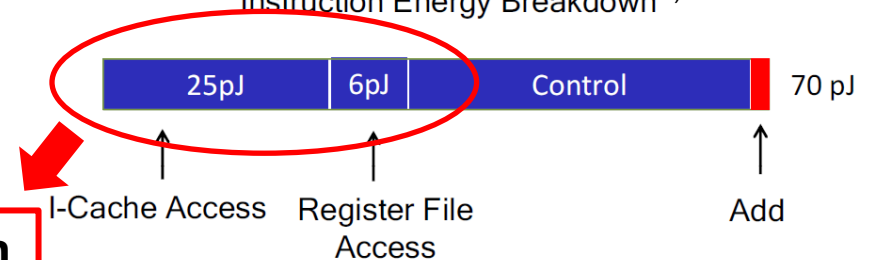


Communication energy efficiency trend ¹⁾



~30% of energy for communication

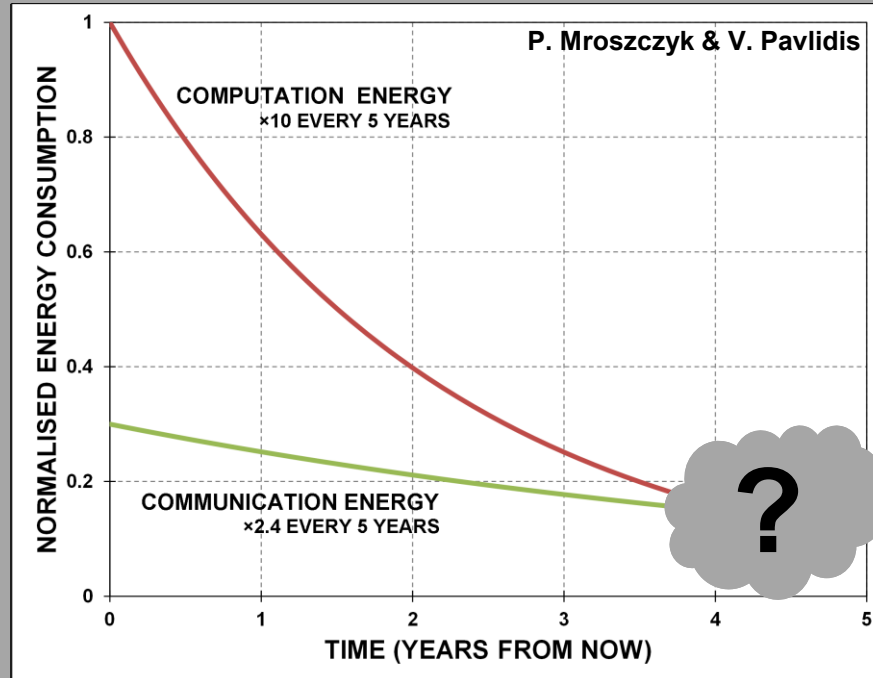
Instruction Energy Breakdown ²⁾



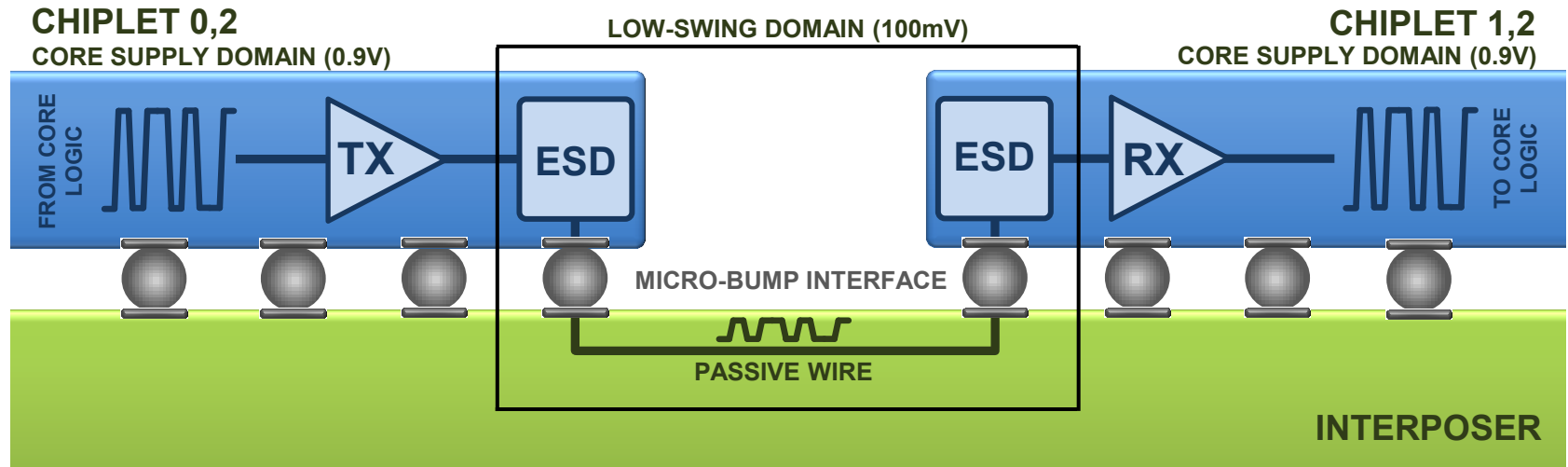
¹⁾ H. Tamura, "Looking to the Future: Projected Requirements for Wireline Communications Technology", IEEE Solid-State Circuits Magazine, Vol. 7, No 4, pp. 53 – 62, 2015.

²⁾ M. Horowitz, "Computing's energy problem (and what we can do about it)", IEEE International Solid-State Circuits Conference, pp. 10 – 14, Mar. 2014

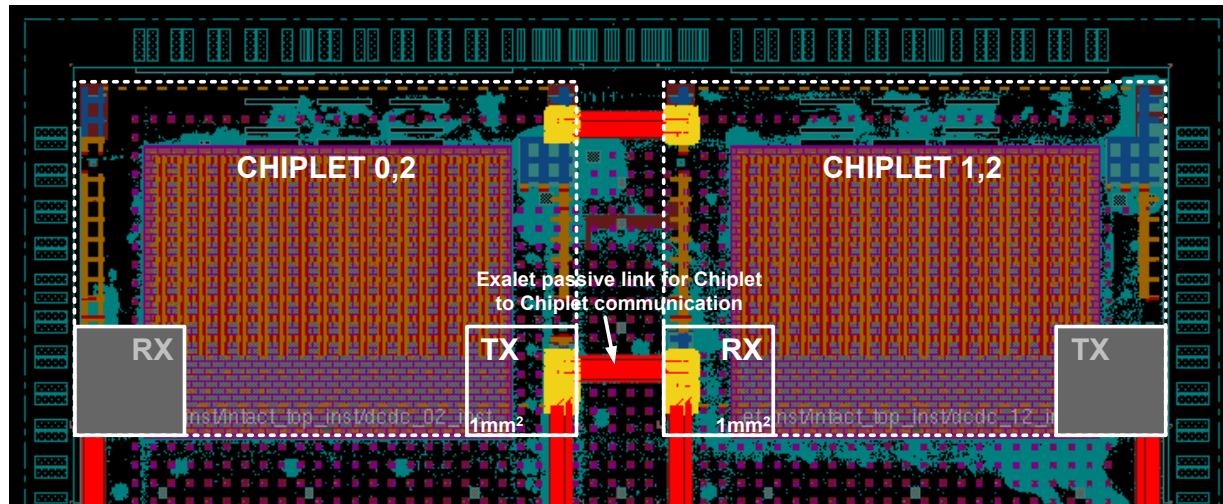
Why Communication matters?



2.5-D Chiplet to Chiplet Physical Interconnect



Cross section of the interconnect with single-ended low swing I/O interface



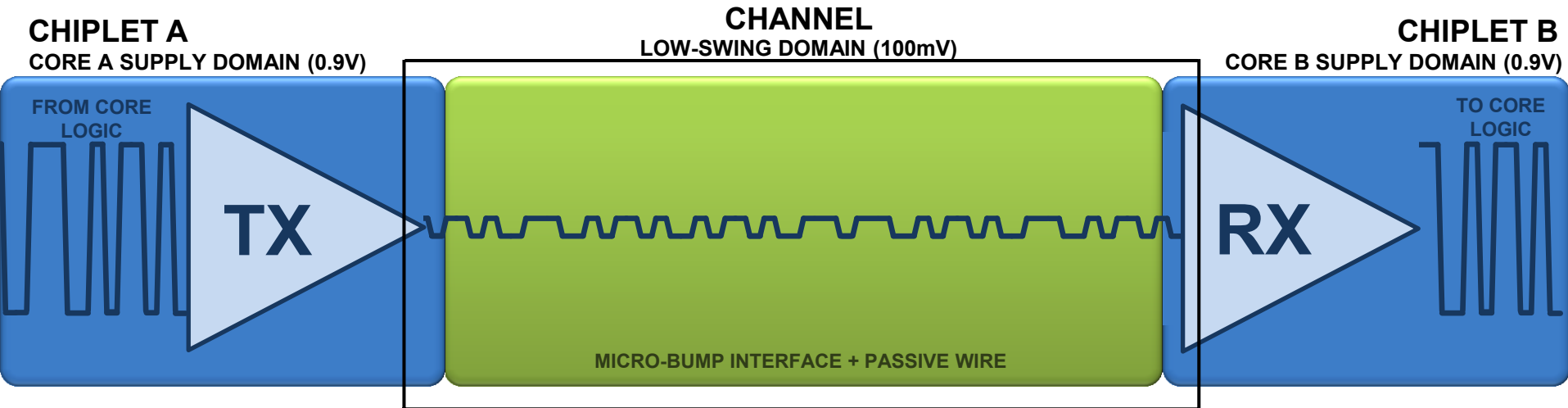
Physical view of the interposer with the projected location of the transceiver and the passive link

Low Swing Signaling Scheme

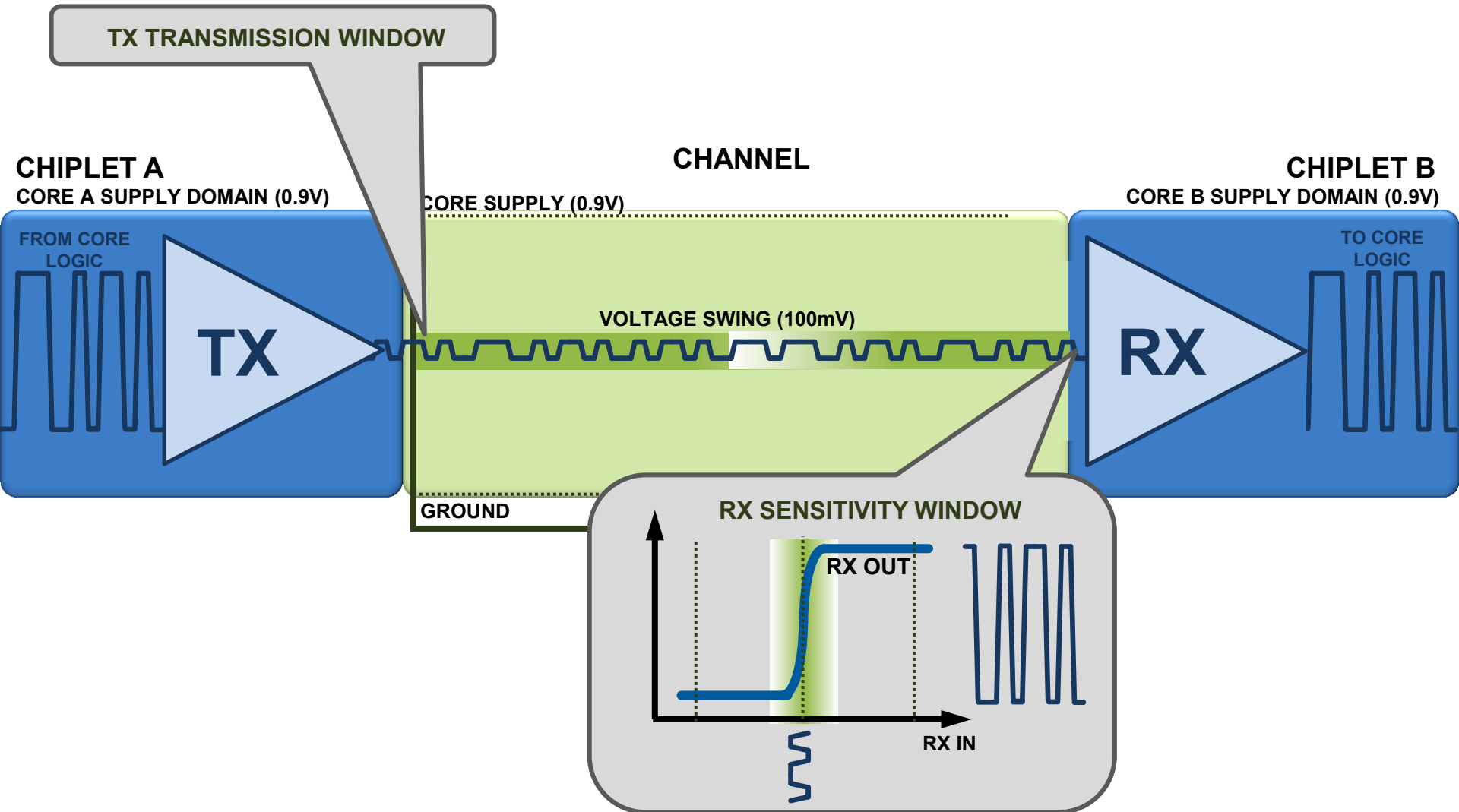
$$\text{ENERGY} \sim \text{DISTANCE} \times \text{VOLTAGE}^2$$



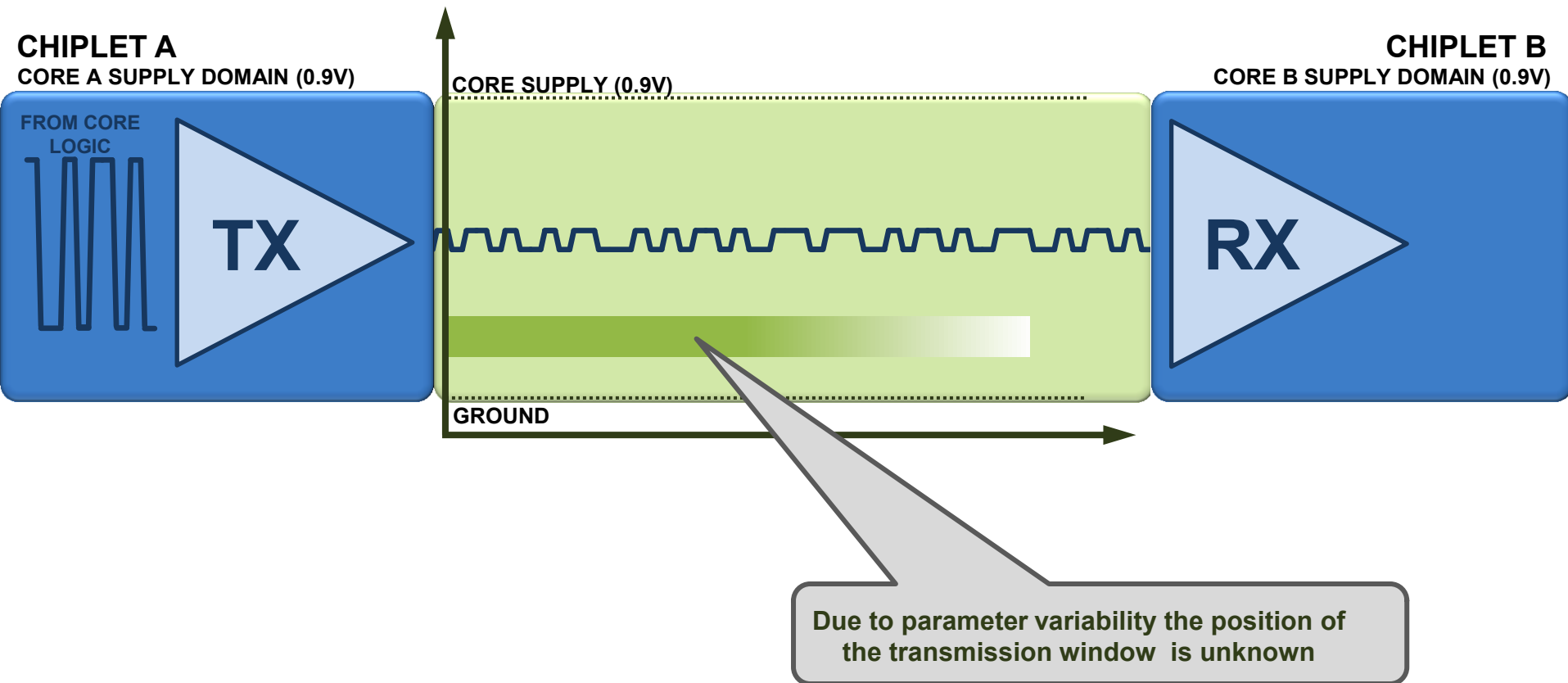
Low Swing



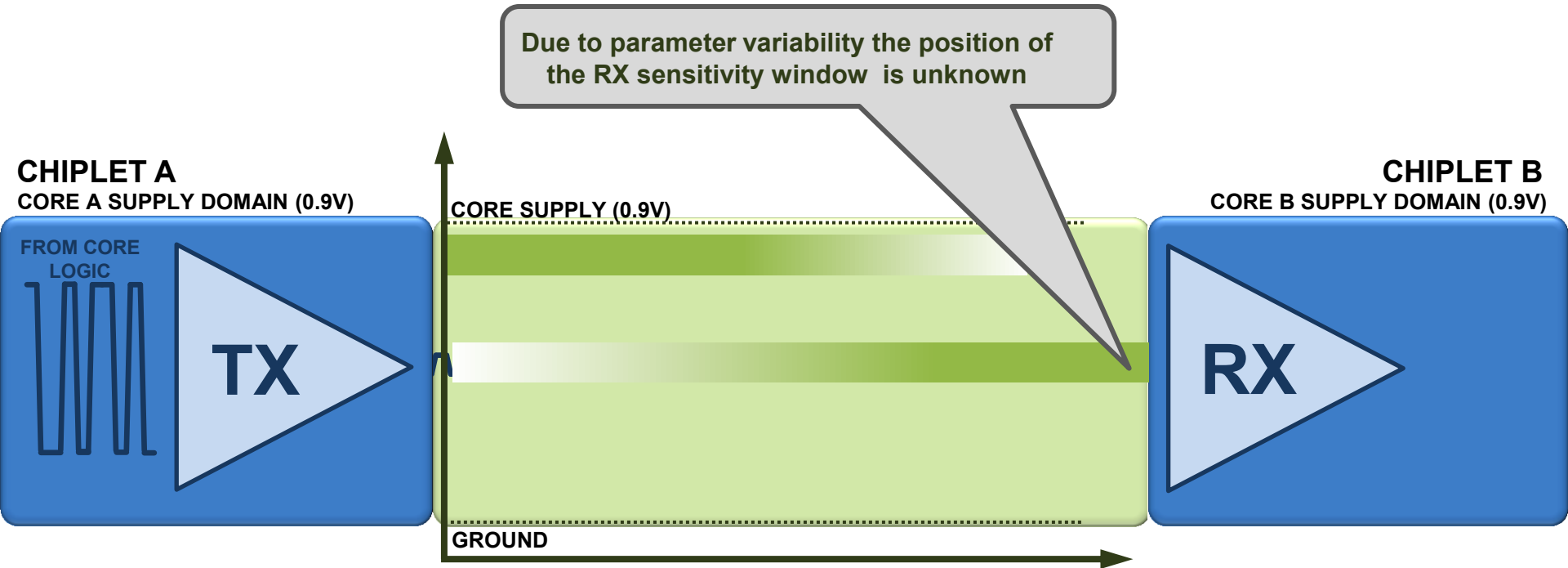
Transmitter and Receiver Design



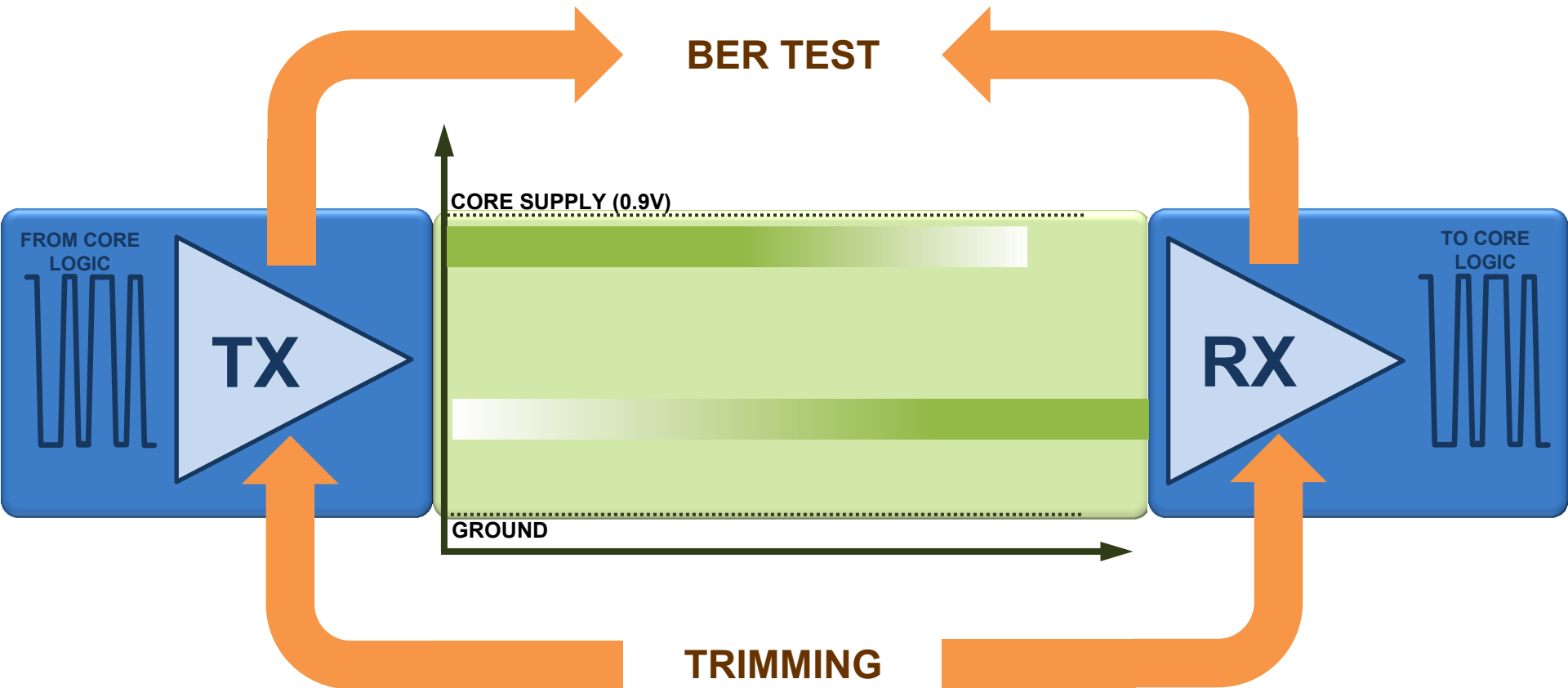
Parameter Variability in TX



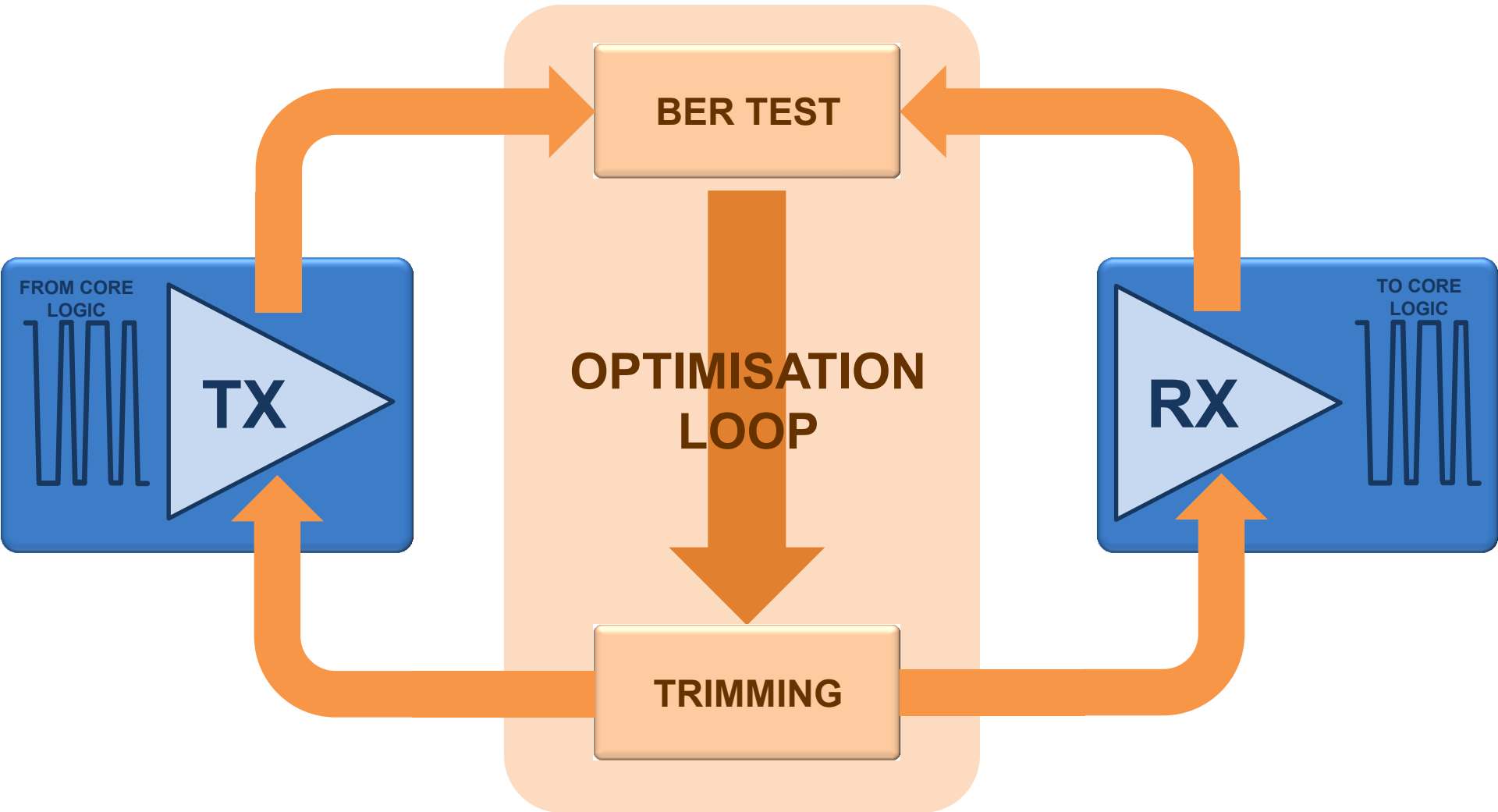
Parameter Variability in RX



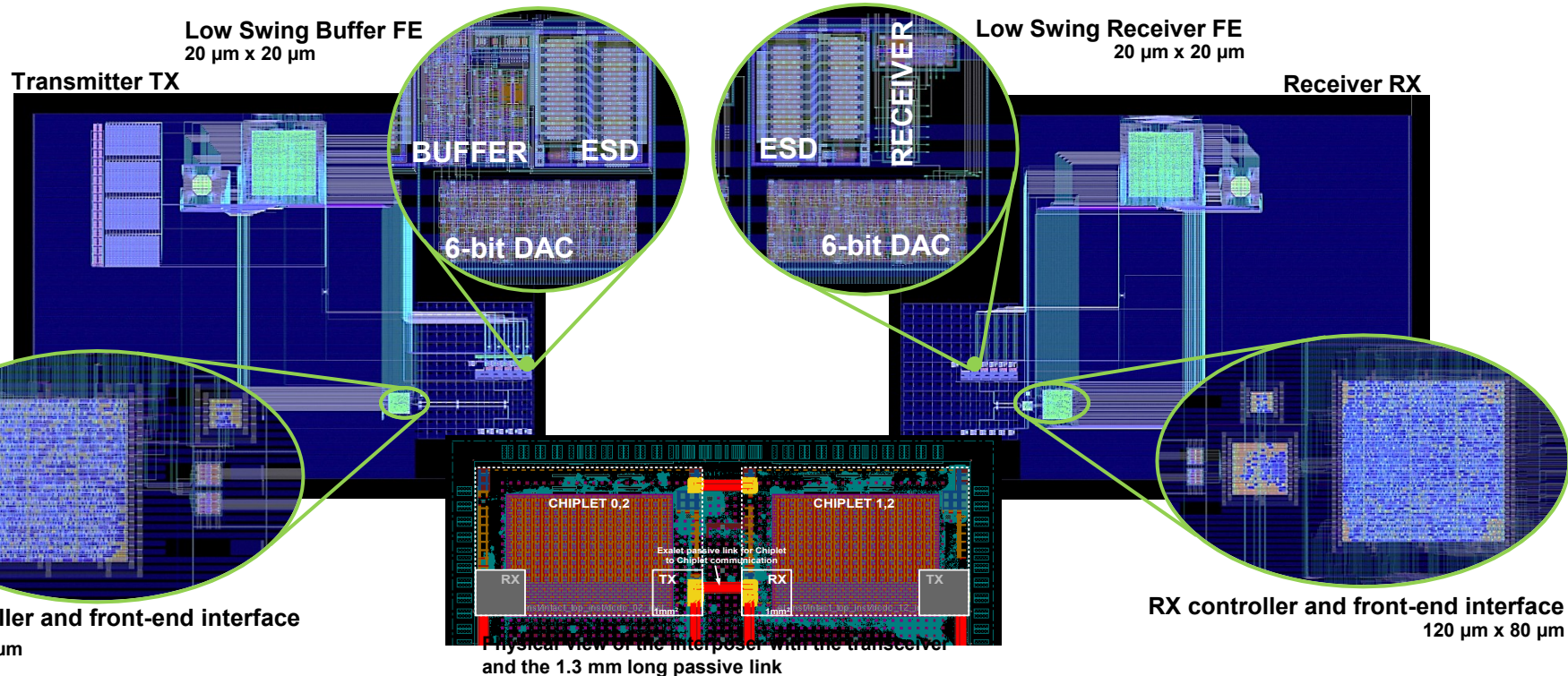
Transceiver Trimming



Transceiver Optimization



EMI v1.0 Transceiver in 28nm FDSOI

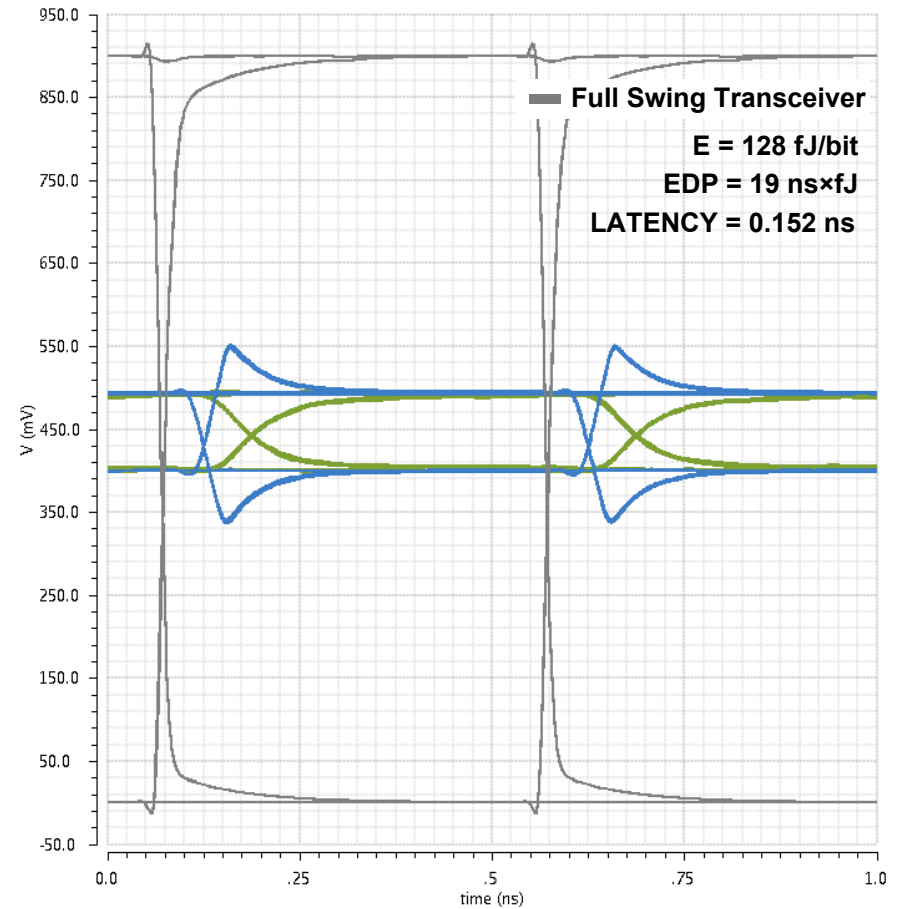
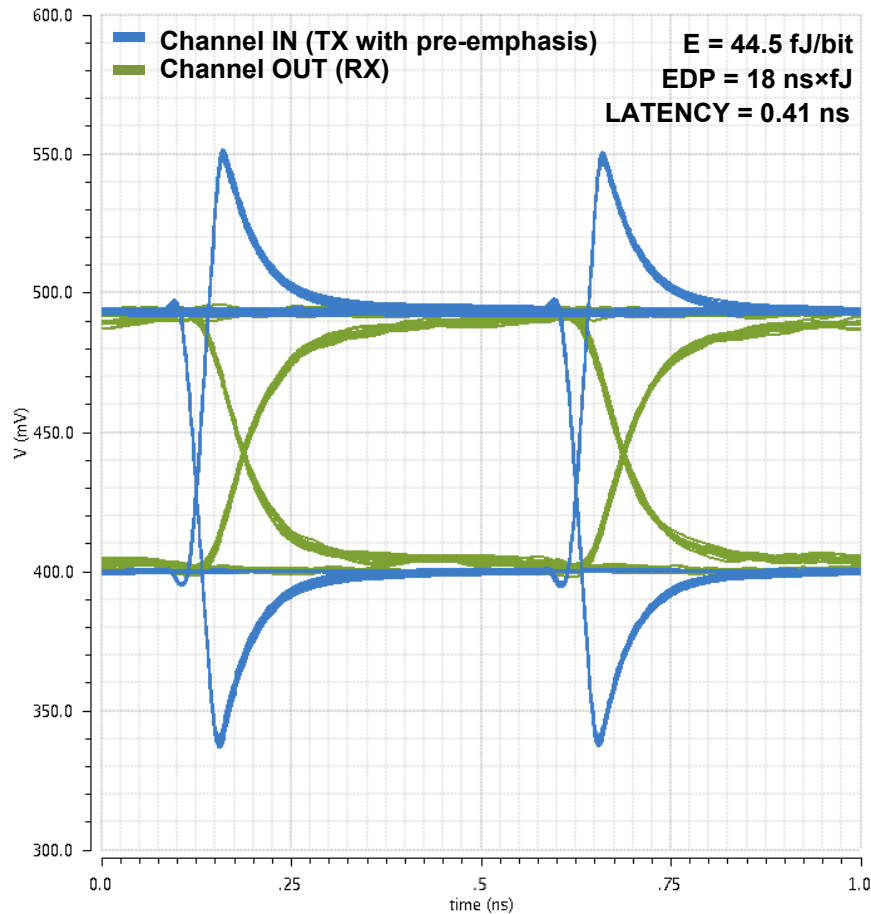


■ Exascale Manchester Interconnect (EMI) v1.0:

- Energy: **44.5 fJ/bit**, Speed: **2 Gb/s/wire** (SDR), bandwidth: **256 Gb/s** (128-wire link), **5 Tb/s/mm²**
- Advanced body biasing scheme for parameter variability trimming
- Up to **3× less power consumption** compared to a standard full swing solution (< 0.1 pJ/bit)
- Over **5× less switching noise** compared to a standard full swing solution
- Latency: 2 clock cycles from TX to RX (0.41 ns for level conversion and signal propagation)

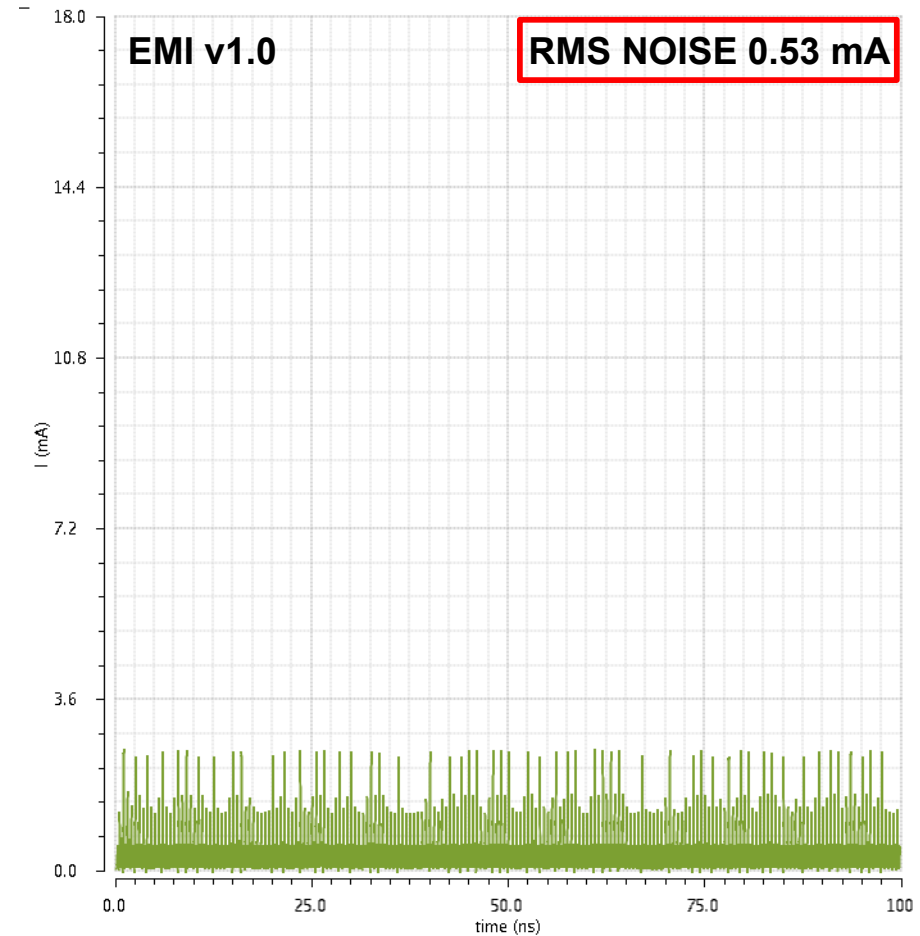
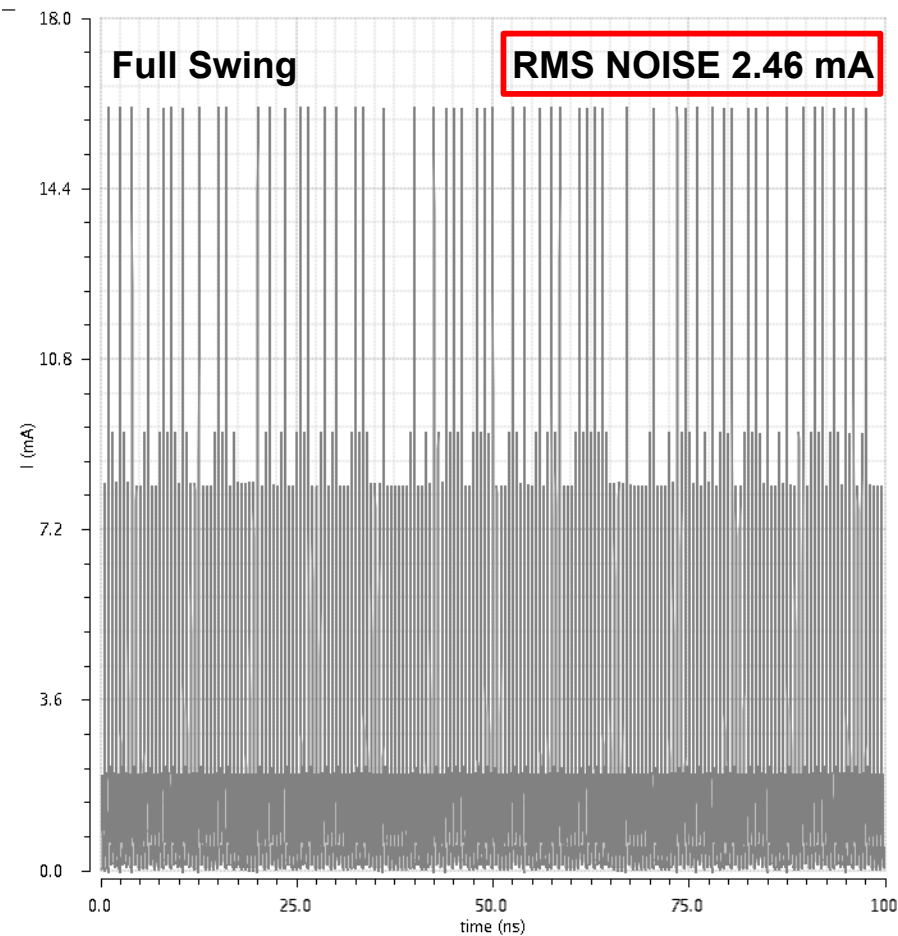
EMI v1.0 in 28nm FDSOI with ExaLet (1.3mm)

1-bit line @ 2 Gb/s (clock shielding) – EYE DIAGRAM

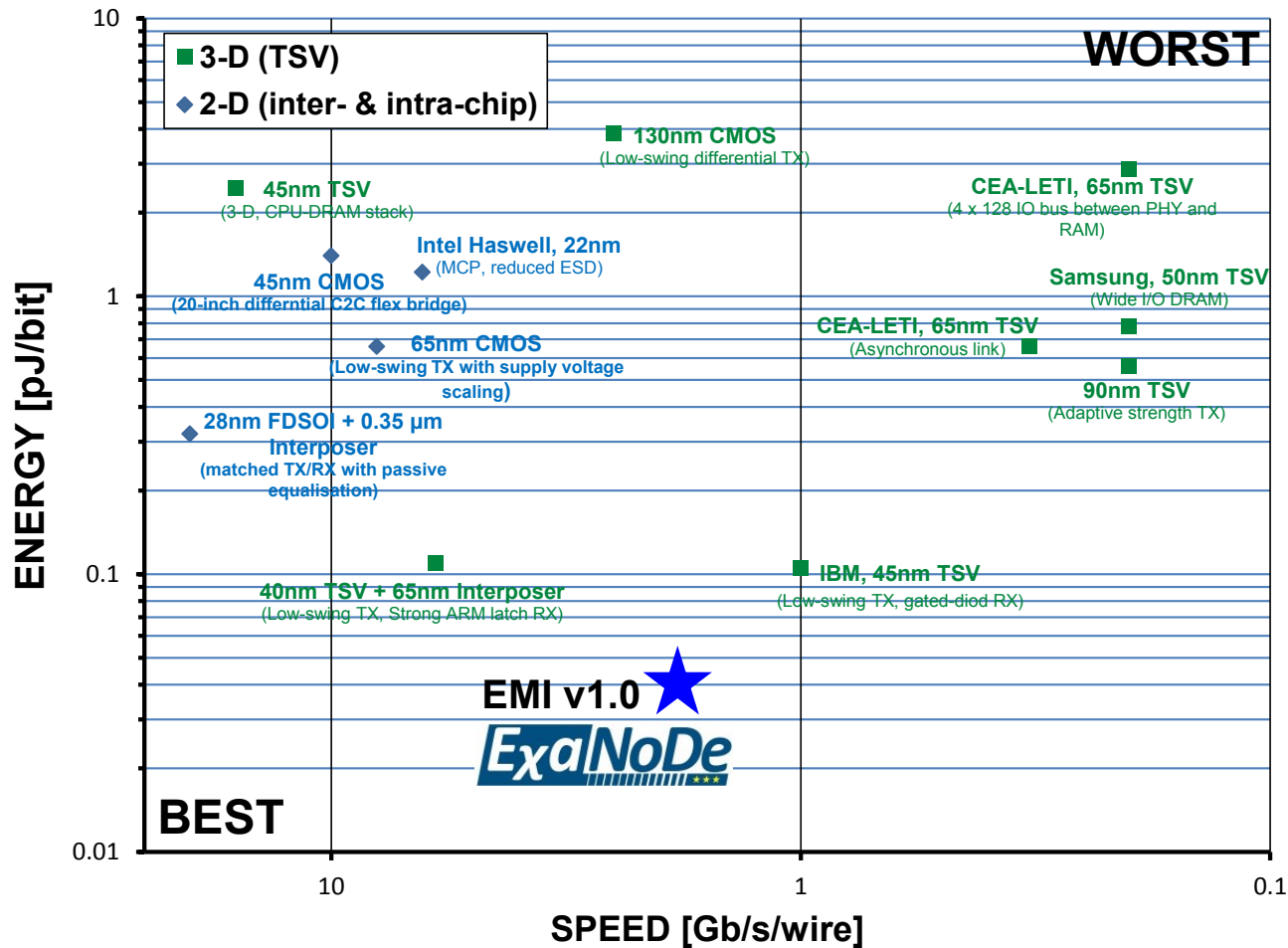


EMI v1.0 in 28nm FDSOI with ExaLet (1.3mm)

1-bit line @ 2 Gb/s (clock shielding) – SWITCHING NOISE



EMI v1.0 Energy Efficiency vs Speed



EMI v1.0 Energy Efficiency vs Area

