Welcome!

European Exascale Processor & Memory Node Design

This project has received funding from the European Union's Horizon 2020 research and innovation programme under grant agreement No 671578

3D-IC design solutions for modular integration of chiplet over silicon interposer

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CEA-LETI

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HiPEAC workshop: Towards Exascale HPC: the ExaNoDe, ExaNeSt, EcoScale, and EuroEXA projects

Outline

- **Advanced Packaging Integration:**
  - Technologies
  - European project landscape
  - High Performance Computing case
  - ExaNoDe Advanced Packaging Technologies
- **3D Integrated Circuit Design Solutions:**
  - ExaNoDe prototype assembly hierarchy
  - Chiplet Architecture & Design
  - Chiplet over Interposer Integration
- **Multi-Chip-Module Challenges and Solutions:**
  - Placement and Routing
  - Assembly Process
- **Conclusion**

Advanced Packaging Integration

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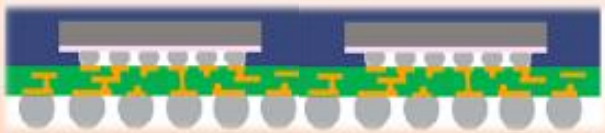
Advanced Packaging Integration: Technologies

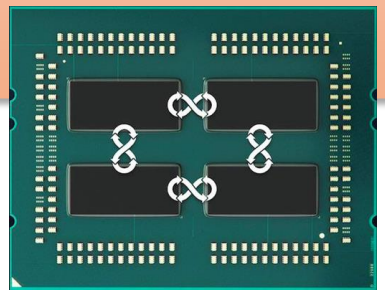
Advanced Packaging Integration

SiP

Multi-Chip-Module



Interconnect density: 100µm x 100µm

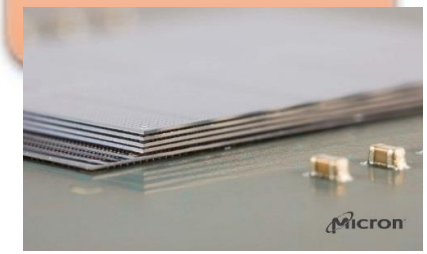


AMD EPYC 7260, 4-chiplet chip

3D

Die stacking

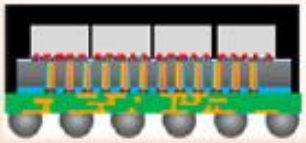
Interconnect density: 10µm x 10µm



Micron High-Bandwidth-Memory

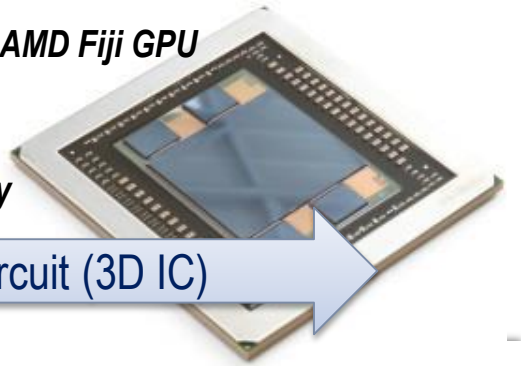
2.5D

Interposer based



Interconnect density: 10µm x 10µm

AMD Fiji GPU

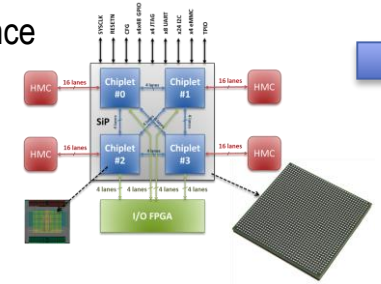


System-in-Package

3D Integrated-Circuit (3D IC)

Advanced Packaging among European HPC Projects

MCM reference design

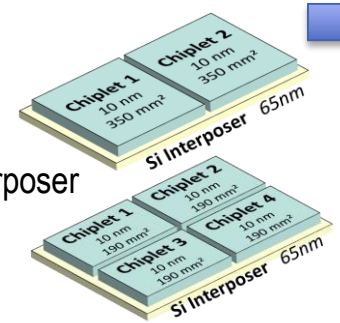


EURO SERVER

MICRO-SERVER

Multi-Chip-Module

Combined architecture / silicon interposer exploration

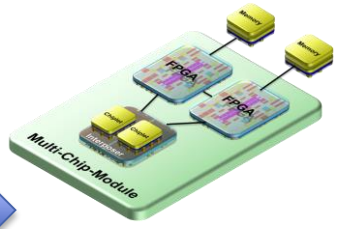


MONT BLANC

HPC

Silicon Interposer

Integrated prototype



HPC

Multi-Chip-Module

Silicon Interposer

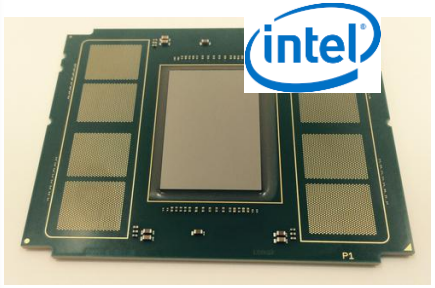
ExaNoDe

Advanced packaging ready for next generation HPC systems

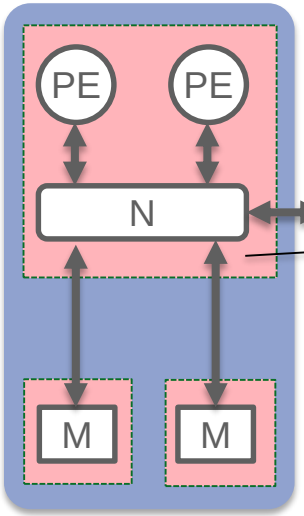
2011-2016 | 2015-2018 | 2018…

Advanced Packaging Technologies for HPC

PROCESSOR

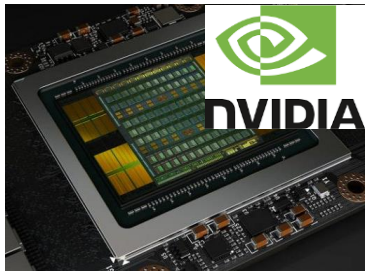


Die-on-Substrate

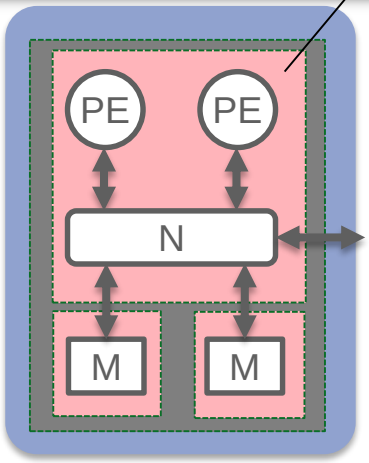


Large die: complex design, high NRE, low yield, high cost

ACCELERATOR



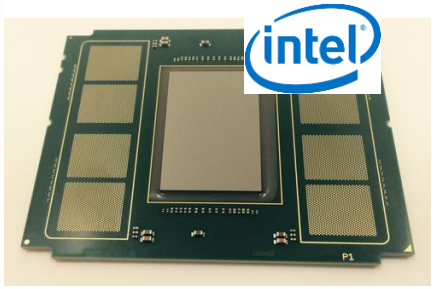
Die-on-Interposer-on-Substrate



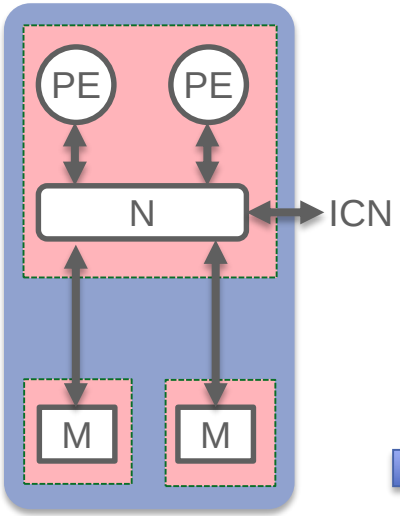
Heterogeneity only possible at board level: high power consumption

Advanced Packaging Technologies for HPC

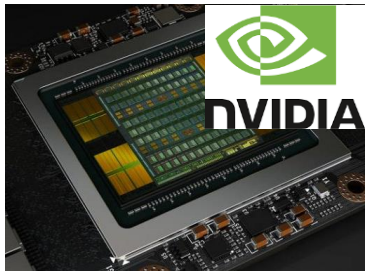
PROCESSOR



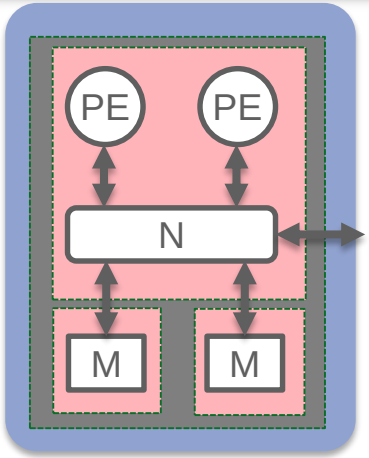
Die-on-Substrate



ACCELERATOR



Die-on-Interposer-on-Substrate

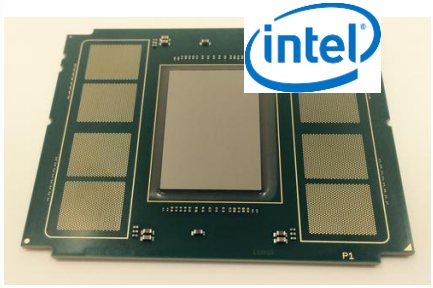


NEXT GENERATION HETEROGENEOUS COMPUTING

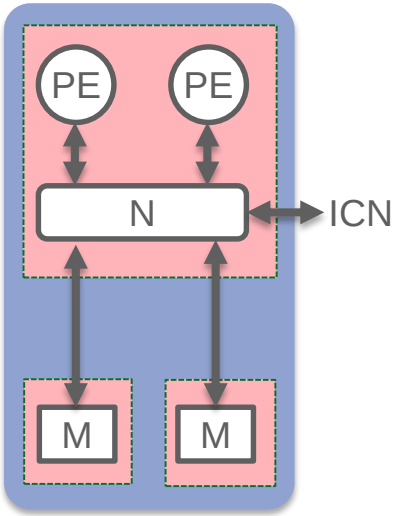
Advanced packaging technologies for low power, low cost and modularity

ExaNoDe Advanced Packaging Technologies

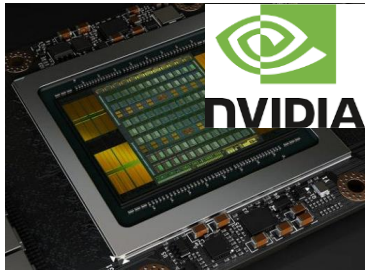
PROCESSOR



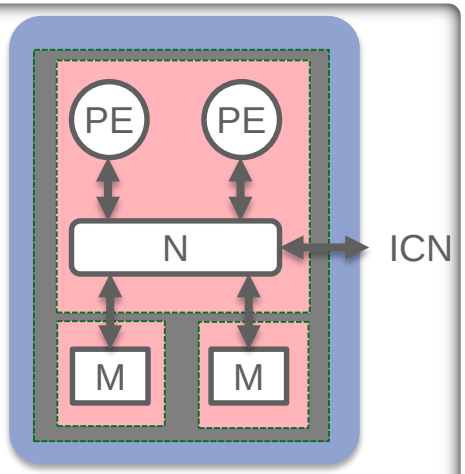
Die-on-Substrate



ACCELERATOR



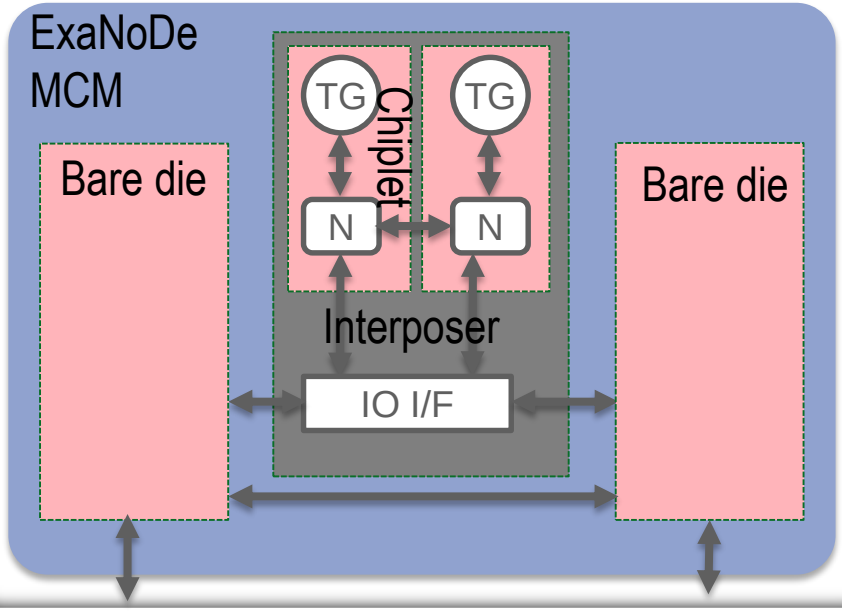
Die-on-Interposer-on-Substrate



HETEROGENEOUS AND MODULAR COMPUTING

ExaNoDe

- *Die-on-Substrate*
- *Large die partitioning: chiplet design*
  - *Chiplet-to-chiplet and chiplet-to-interposer high speed links*
- *Chiplet-on-Interposer-on-Substrate*



3D Integrated Circuit Design Solutions

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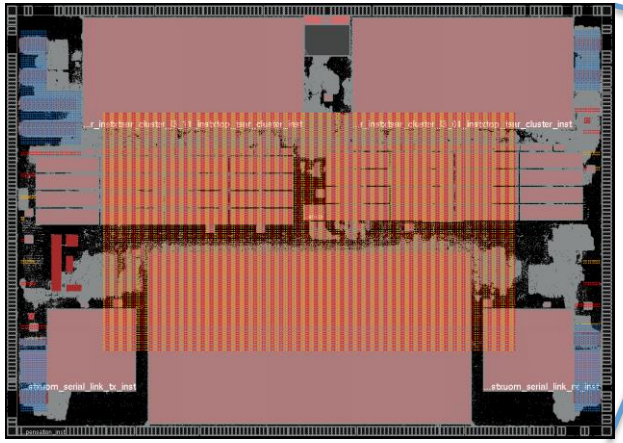
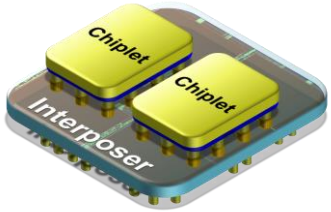
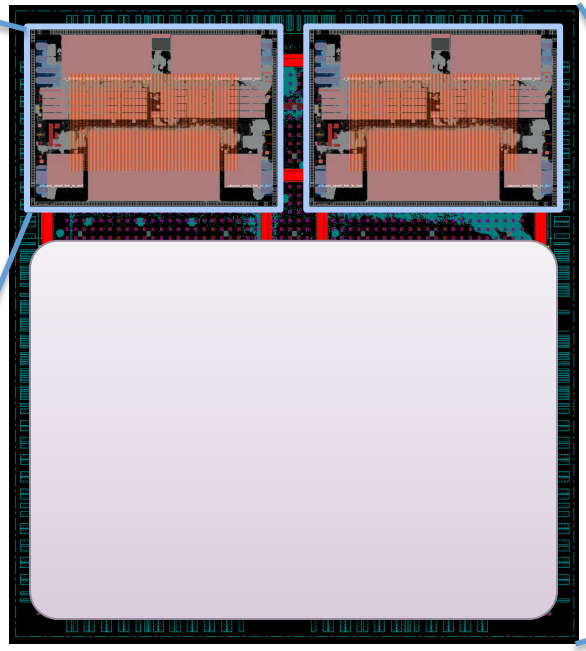
ExaNoDe Assembly Hierarchy

Chiplet

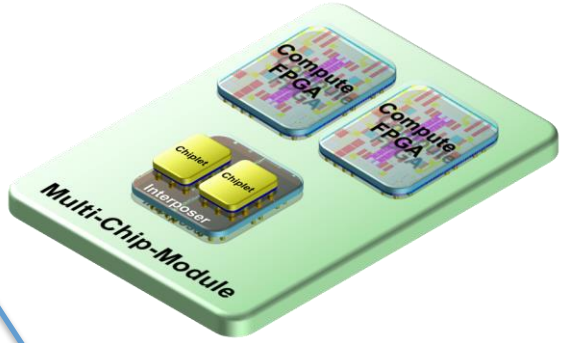


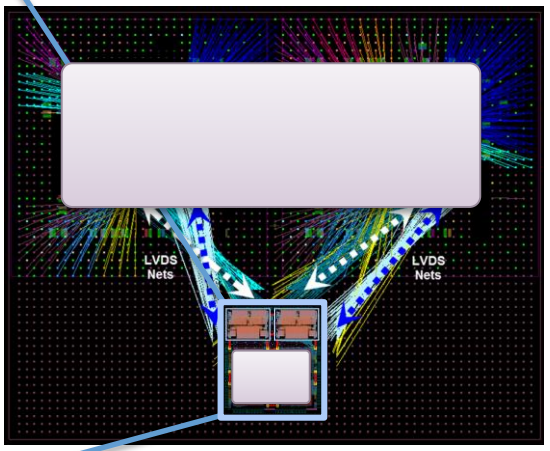
Interposer



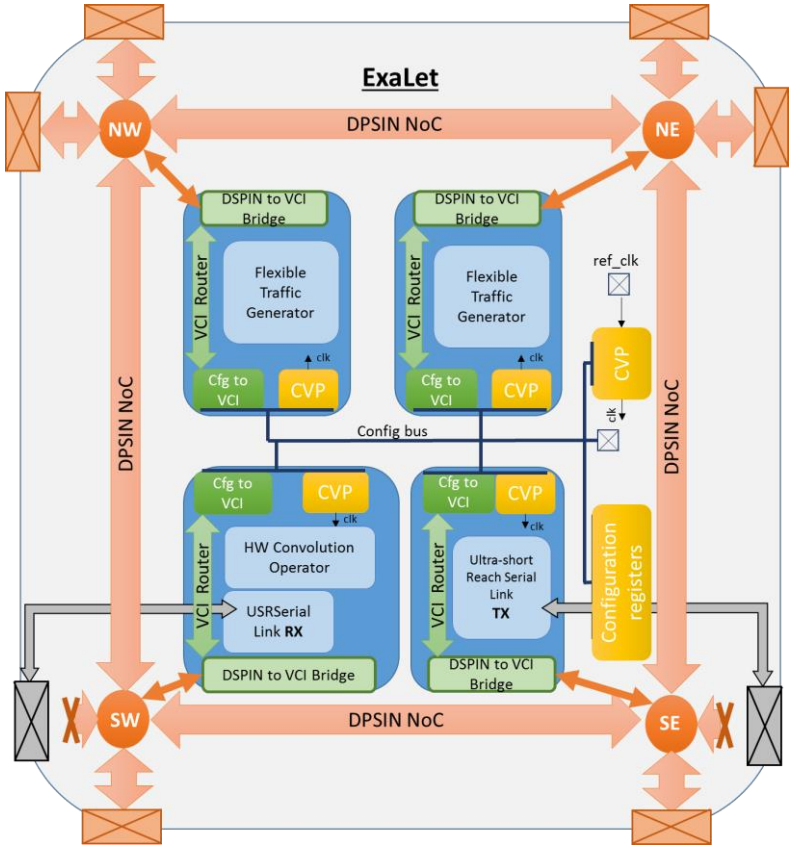


Multi-Chip-Module



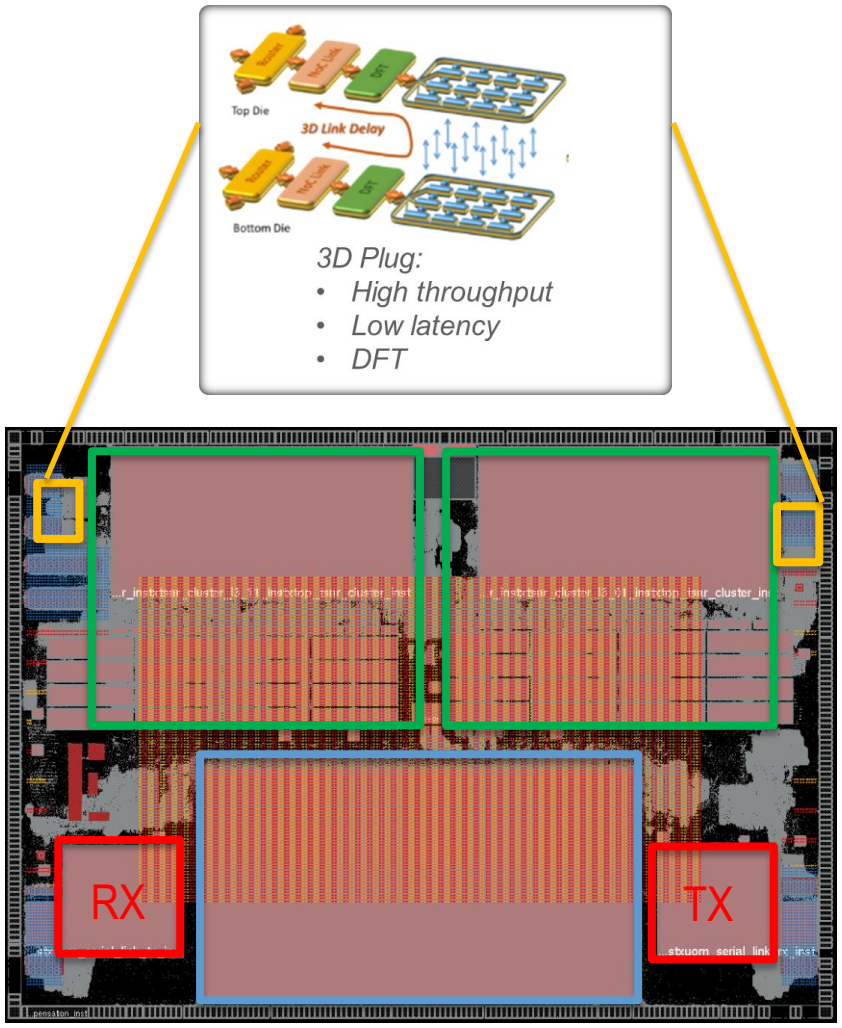


Chiplet Architecture



- **Programmable Traffic generator (CEA)**
- **Ultra Short Reach chiplet-to-chiplet fast serial link (UOM)**
  - Mapping over the160 passive link available
- **Convolutional Neural Networks (ETHZ)**
- **Bridge VCI <--> AXI (CEA/ETHZ)**
- **DSPIN Network on chip and 3D plug (CEA)**
  - communication between clusters and inter-chiplet
- **FLL**

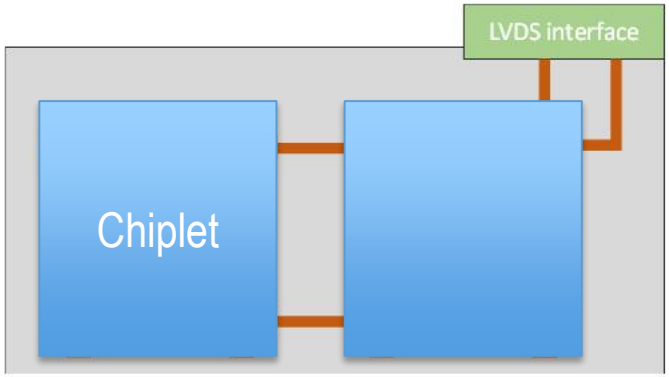
Chiplet Design

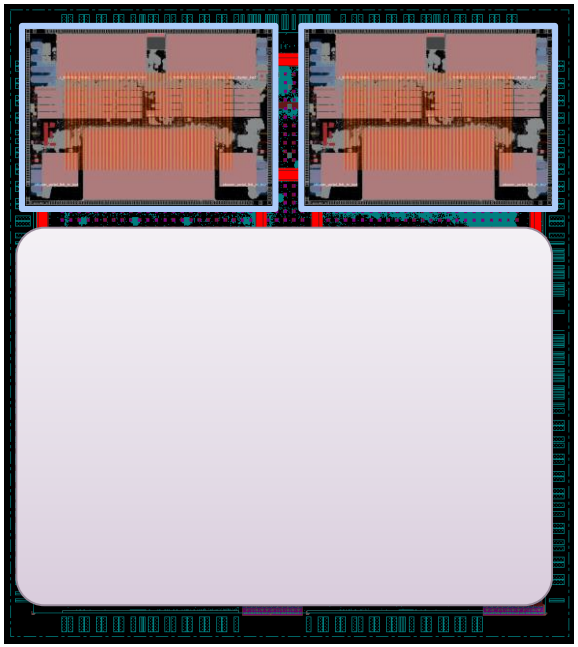


- **28FDSOI STM process**
- **Tape out on June 7th, 2017**
- **Timing closed over the full window of the process variation defined by the foundry**
- **Wafers back from fab end of 2017**
  - Ready for 3D bump growth steps

- Convolutional Neural Networks (ETHZ)
- Programmable Traffic generator (CEA)
- Ultra Short Reach chiplet to chiplet fast serial link (UOM)

Chiplet over Interposer Integration





- **3D Integrated Circuit:**
  - Chiplet design with communication infrastructure and HW accelerators.
  - Interposer design with FPGA interface.
  - Chiplet to chiplet high speed serial link communication
  - Multi-level global interconnect
  - Embedded DC-DC on the interposer for chiplet supply voltage adjustment

Multi-Chip-Module Challenges and Solutions

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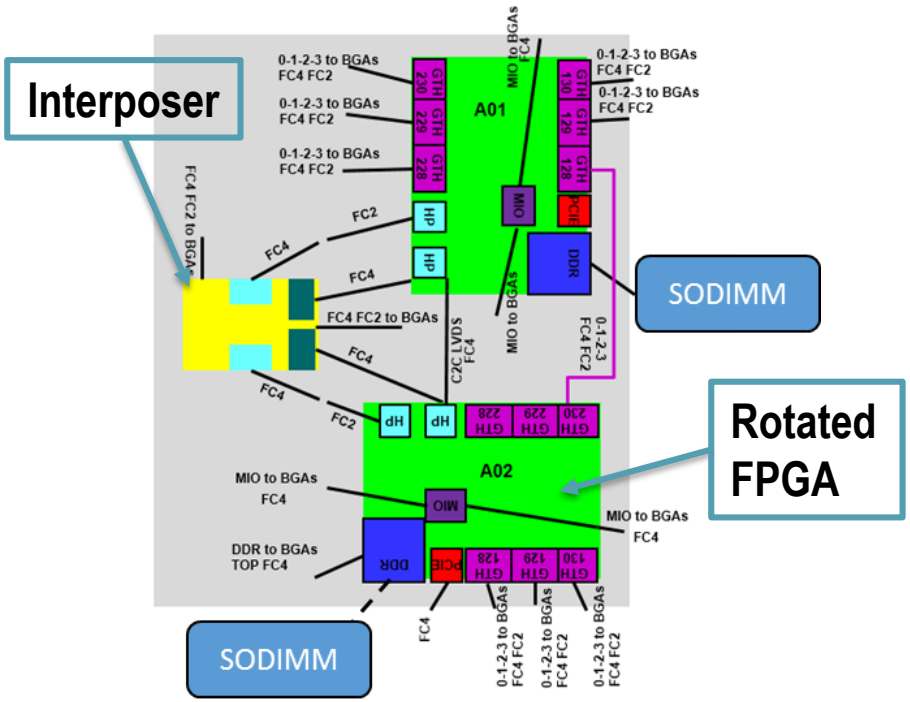
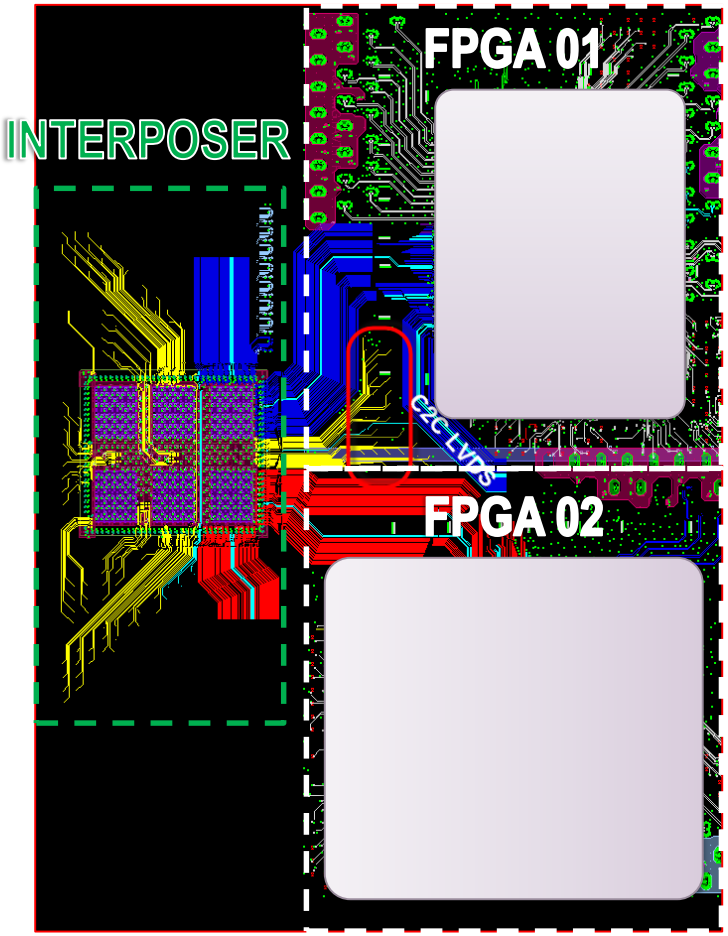
Multi-Chip-Module Challenges and Solutions

- **MCM components positioning and routing**

FPGA orientation and bank assignations optimized to reduce LVDS crossings and allow SODIMM connection (board level)

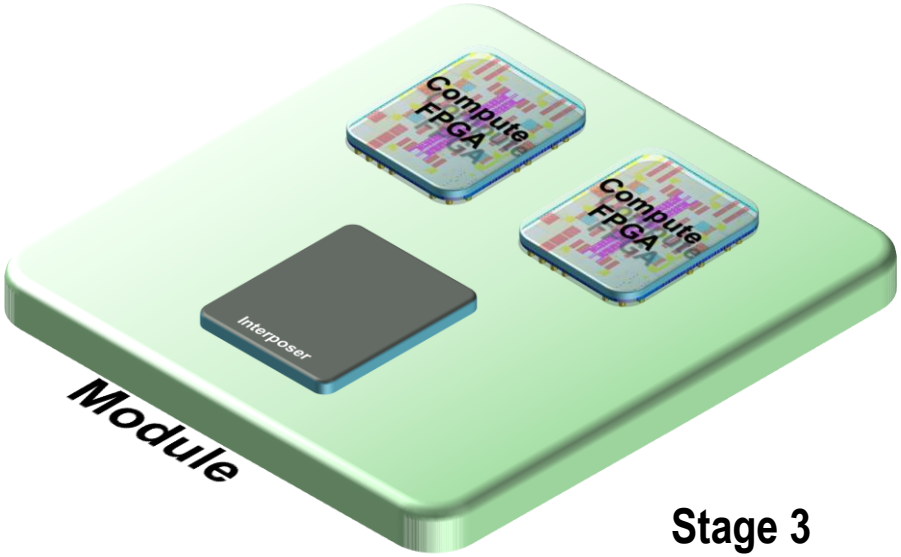




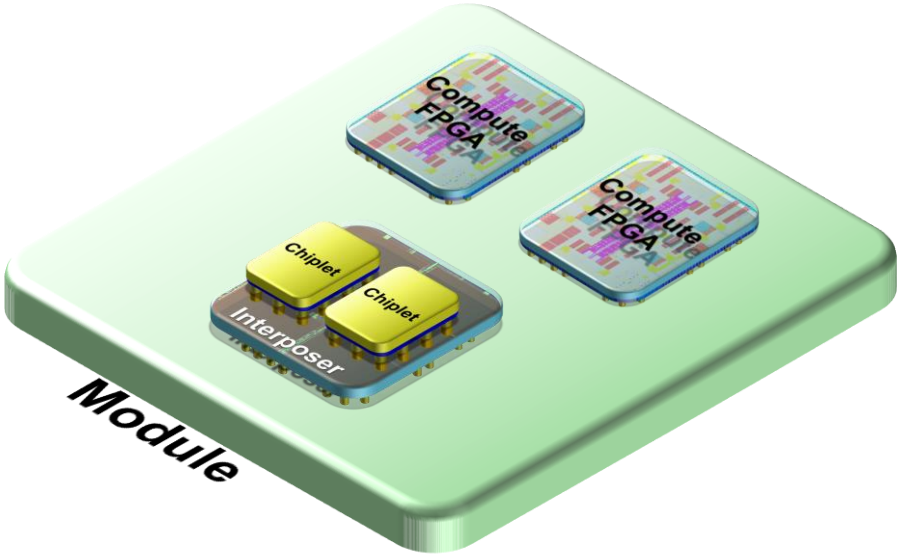
Multi-Chip-Module Challenges and Solutions

- **MCM assembly process**

Stage 1
- Decoupling capacitors, FPGAs and interposer placement (pick & place, flip chip)
- Mass reflow



Stage 2
- Chiplets stacking on interposer by thermocompression bonding



Stage 3
- Copper lid placement
- BGA placement and reflow

Conclusion

- **Advanced Packaging:**
  - a key enabling technology for high performance and power efficient processors and accelerators.

- **ExaNoDe main innovations related to advanced packaging:**
  - 3D Integrated Circuit design solutions,
  - Ultra Short Reach chiplet-to-chiplet fast serial link,
  - 3D plug for chiplet-to-interposer wide data link,
  - Chiplet-on-Interposer-on-MCM assembly process.

- **ExaNoDe advanced packaging enables:**
  - modularity thanks to chiplet design solutions,
  - power efficient heterogeneity with Chiplet-on-Interposer-on-MCM assembly process.

Acknowledgements:

This project has received funding from the European Union's Horizon 2020 research and innovation programme under grant agreement No 671578

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Thank you!

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