



D6.2 Dissemination strategy Document

Workpackage:	6	Dissemination and Exploitation
Author(s):	Christian Pinto	VOSYS
	Daniel Raho	VOSYS
Authorized by	Christian Pinto	VOSYS
Reviewer	Francis Wray	SCAPOS
Reviewer	Annaïk Colliot	BULL
Reviewer	Denis Dutoit	CEA
Dissemination Level	Public	

Date	Author	Comments	Version	Status
2015-11-12	C. Pinto	Initial draft	V0.0	Draft
2015-11-13	C. Pinto, D. Raho	Populated sections	V0.1	Draft
2015-11-16	C. Pinto, D. Raho	Initial text, fixed typos	V0.2	Draft
2015-23-11	V. Subotic	Added BSC input on Memory technology and parallel programming models	V0.3	Draft
2015-27-11	C. Pinto, D. Raho	Added VOSYS contribution on virtualization, added Dissemination actions, general edits.	V1.0	Draft
2015-11-30	M. Katevenis, M. Marazakis	Added content on systems s/w dissemination	V1.1	Draft
2015-12-1	D. Dutoit	Added CEA Contribution	V1.2	Draft
2015-12-01	C. Pinto, D. Raho	Integrated CEA Contribution, final draft.	V2.0	Final Draft
2015-12-01	A. Colliot	Document Review	V2.1	Final Draft
2015-12-01	D. Dutoit	Document Review	V2.2	Final Draft

2015-12-01	C. Pinto, D. Raho	Document modified according to reviews from Annaik Colliot and Denis Dutoit	V3.0	Final Draft
2015-12-01	A. Colliot, D. Dutoit, F. Wray	Feedback from internal review panel	V3.1	Final Draft
2015-12-11	C. Pinto, D. Raho	Integration of Consolidated review.	V4.0	Final Draft
2015-12-14	C. Pinto, D. Raho	Final text review, removed extra line feeds.	V4.1	Final Version

Executive Summary

Among the primary goals of the European Commission funding schemes, aiming at ensuring the European strategic position on target technical fields, there is a need to maximize the impact of projects. The project's dissemination activity is designed to overcome various societal, economical and scientific challenges. In addition, the dissemination activity is considered as the vehicle for innovation. Its aim is not only to develop a publicly visible outcome for the scientific community, but also to demonstrate industrial applicability. The research and the performed development work will generate foreground with concrete industrial applicability, and possibly be available in next generation off-the-shelf products.

In the ExaNoDe project, the partners plan to give great importance to dissemination by publishing scientific papers to international conferences or journals, by participating to events organized by the European community, by joining various European projects from correlated domains, and by contributing to the OpenSource software development community and to standards whenever possible, as for example OpenMP.

The present document describes the dissemination strategy decided for the ExaNoDe consortium: definition of a project website, logo and flyer, regular press releases through partner websites and/or relevant publishers, main target conferences and journals for scientific publications, and the organization of a workshop. The ExaNoDe consortium has identified a set of dissemination actions, with specific stakeholders and a metric to measure the impact of the actions taken.

The document outlines also a set of dissemination groups, linked to the different technical areas touched by the project, each of them having a different dissemination audience. Target conferences and stakeholders are described for each dissemination group.

Table of Contents

1	Introduction	1
2	Project identity: website, logo, flyers and social media presence	2
3	Press releases	3
4	Scientific publications	3
4.1	International conferences and journals	3
4.2	Open-access to publications	5
5	Contribution to standards	5
6	Organization of a workshop	6
7	Dissemination of software and applications.....	6
8	Dissemination actions.....	6
9	Dissemination groups	8
9.1	Silicon interposer design and manufacturing	8
9.2	Memory Technology	8
9.3	System Software	9
9.4	Parallel Programming Models and runtimes	10
9.5	Virtualization of system and resources.....	11
10	Concluding Remarks	12
11	ANNEX A: Poster presented at Supercomputing 2015	13
12	Glossary.....	14

List of abbreviations

ACM	Association for Computing Machinery
DDR	Double Data Rate
DMP	Data Management Plan
EC	European Commission
ECC	Error Correcting Code
ECTC	Electronic Components and Technology Conference
ETP4HPC	European Technology Platform for High-Performance Computing
ExaNoDe	European Exascale Processor Memory Node Design
GPI	Global Address Space Programming Interface
HPC	High Performance Computing
ICT	Information and Communication Technology
IMAPS	International Microelectronics Assembly and Packaging Society
IEEE	Institute of Electrical and Electronics Engineers
IPR	Intellectual Property
KVM	Kernel-based Virtual Machine
LPDDR	Low-Power Double Data Rate
MPI	Message Passing Interface
NIC	Network Interface Controller
NVM	Non Volatile Memory
PGAS	Partitioned Global Address Space
QEMU	Quick EMUlator
RDMA	Remote Direct Memory Access
SEO	Search Engine Optimizer
SRA	Strategic Research Agenda
TSV	Through Silicon Via
UEFI	Unified Extensible Firmware Interface
WP	Work Package

1 Introduction

This deliverable provides a description of the strategy adopted by the ExaNoDe consortium to guarantee a successful dissemination of the outcomes of the project. The dissemination and exploitation lifecycle of this European project can be divided in three main phases (Figure 1), spanning over the three years of the project and partially overlapping between each other. The three phases are namely:

- Creation and maintenance of the Awareness of the project
- Dissemination of Scientific results
- Exploitation of the results

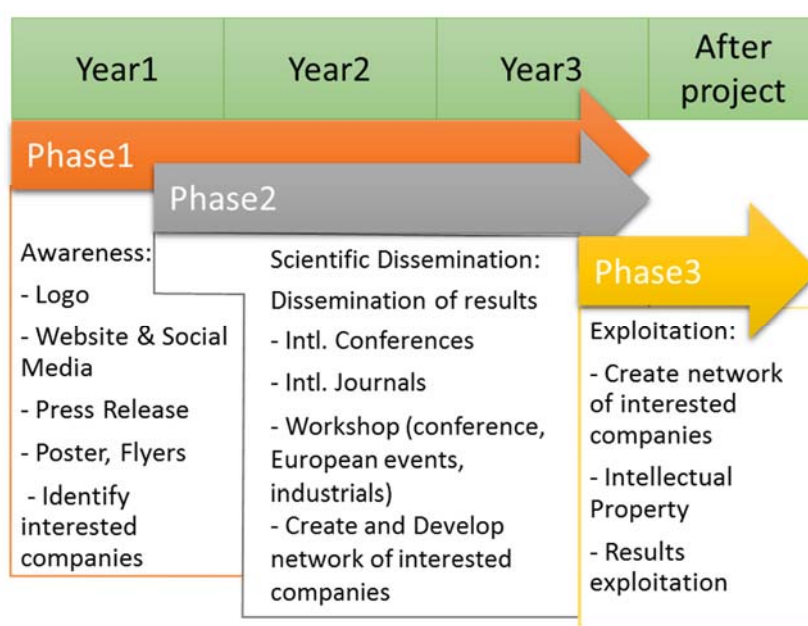


Figure 1: Project dissemination and exploitation phases

Creation and maintenance of the Awareness of the project: The main aim of this phase is to make the public aware of the project. Public stakeholders are the scientific community and industrial entities. At the very beginning of this phase a logo and a website will be designed. The logo will unequivocally identify the project. The website will be designed, as the basic infrastructure for publicizing the project. In addition a poster and flyers describing the goals of the project will be prepared, to be used during international events. The vehicles to create awareness for the project will be maintained and updated throughout the duration of the project, ensuring a knowledgeable and continual presentation of the project at relevant events or in front of companies that could be interested by the project. New developments will be advertised by releasing periodic press releases.

Dissemination of Scientific results: The main tool for the dissemination of the results of this research project is scientific publications, whose aim is twofold on one hand to share with the

community the outcomes of the research, and on the other hand to get feedback about the research direction, which is going to fulfil the requirements of potential exploitations. Within the ExaNoDe project the consortium plans to perform a continuous dissemination with the organization of a workshop, and the publication of conference and journal papers.

In addition the consortium will create and develop a network of companies interested in the ExaNoDe project (Industrial advisory board) technology that in the third phase will be used to maximize the possibilities for commercial exploitation of the project innovations.

Exploitation of the results: This third phase starts close to the end of the project, and continues after its end. Exploitation is cited in this document only for completeness, and to enforce that a good dissemination plan (phases 1 and 2) will increase the visibility of the work done, while highlighting the strengths of the introduced innovations.

Therefore, the aim of the present document is to give the preliminary details and plans related to Phase1 and Phase2 (Figure 1) for the ExaNoDe project.

2 Project identity: website, logo, flyers and social media presence

In the digital era it is of extreme importance to have a viral presence on the web, to maximize the size of the audience caught by the information shared. Seamlessly, this is true for a research project as the second major factor of success is the creation of awareness and the pervasive dissemination of the results.

The ExaNoDe project will be present on the web by means of a website, providing to public users general information about the project goals and ambitions, the partners involved, the list of the publications, and a main contact to be used in case further information are needed. Such a website will take into account the implementation of SEO (Search Engine Optimizer) techniques and continuous content publication with the intent of maximizing the visibility through search engines.

In addition to the website the consortium foresees the creation of dedicated social media (e.g., Twitter, LinkedIn) accounts for the ExaNoDe project, to further improve the amount of information spread across the web.

In addition, to enforce the identity of the project a logo univocally identifying the project and a flyer will be designed in order to be used, the former as identification mark in every formal/un-formal document, the latter to be used in conferences or other venues where the project participates.

A dedicated deliverable (D6.1) at M3 will take care of all the aspects described in this paragraph.

3 Press releases

The press strategy will be consistent with the dissemination strategy and its objectives. As one of the most relevant press activities, the press strategy will last for the complete duration of the ExaNoDe project. This strategy will also be analysed in more detail at M6 in the Initial Project Press Release Deliverable (D 6.3).

Press releases are one of the most effective ways of communicating the existence of the ExaNoDe project to a specific target audience (general public and related institutions). Press releases attract attention to the project's progress and its achievements. During the project, different press releases will be launched but the initial press release is the most important one because it defines the ExaNoDe project's objectives as well as its working plan. In the middle of the project there will be another press release in order to explain its progress and at the end of the project, a press release for the scientific results. The ExaNoDe final press release, with the scientific results and impact, will be described at M36 in a dedicated deliverable (D6.6).

The Work Package 6 team will prepare a first draft of the press release to announce the launch of the project. This text will be validated by all partners as well as by the Management Team (WP1). Once these steps have been agreed, all partners will also have to agree the launch date and time. Each partner has the responsibility of translating the press release from English into their own local language (German, French, Greek and Spanish) and launched it to the local media by each partner in the project. This will be the procedure to follow to launch all ExaNoDe press releases.

All press releases will be included in the ExaNoDe press corner of the project website. Furthermore, all partners will have the opportunity to include it on their institutional website (example: BSC will include the press release into the press section of the website: <http://www.bsc.es/about-bsc/press/press-releases%20>) in order to increase the click rates. The ExaNoDe website will include all press releases in all languages as well as all press impacts.

4 Scientific publications

4.1 International conferences and journals

Scientific publications are still the primary, and most effective, tool for the dissemination of scientific outcomes generated by any European research project, with ExaNoDe not being an exception. The ExaNoDe consortium has planned to produce about 20 conference presentations, posters and/or keynote talks (at least 10 international) and 5 journal submissions where the following results are expected to be presented:

- a) Energy-efficiency and scalability of the ExaNoDe compute element
- b) Nanotechnology integration approach and results
- c) Results from Everything close to design principle
- d) Compute density and the drive towards exascale
- e) Scalability of HPC application and runtimes
- f) Virtualization techniques applicable to HPC

Following a list of the most relevant target conferences and journals.

International Conferences:

- SC IEEE Supercomputing Conference

- **ISC**, International Supercomputing Conference
- **ICS, ACM International Conference on Supercomputing**
- **DAC** IEEE Design Automation Conference
- **ISCA** IEEE International Symposium of Computer Architecture
- **MICRO** IEEE/ACM International Symposium on Microarchitecture
- **FCCM** IEEE Symposium on Field-Programmable Custom Computing Machines
- **FPL** IEEE Field Programmable Logic Conference
- **SAMOS** IEEE International Symposium on Systems Architectures Modeling and Simulation
- **HiPEAC** Int. Conference on High Performance and Embedded Architectures and Compilation
- **PPoPP**, ACM SIGPLAN symposium on Principles and practice of parallel programming
- **PLDI**, ACM SIGPLAN symposium on Programming Language Design and Implementation
- **PACT**, Parallel Architectures and Compilation Techniques
- **ACM SIGMETRICS**
- **ADASS**, Astronomical Data Analysis Software & Systems
- **IPDPS**, IEEE International Parallel & Distributed Processing Symposium
- **HPCA**, IEEE International Symposium on High-Performance Computer Architecture
- **HPPC** , IEEE - High Performance Computing and Communications
- **CLUSTER**, IEEE - Cluster Computing and Workshops
- **MPSOC** Forum, International forum of industry and academic thought leaders
- **SAAHPC**, IEEE - Application Accelerators in High-Performance Computing
- **ACM SIGMOD** – International conference on Management of Data
- **VLDB** – International conference on Very Large Data
- **DAMON** – International workshop on Database on Modern Hardware
- ACM ASPLOS (Architectural Support for Programming Languages and Operating Systems)
- **USENIX ATC (Annual Technical Conference)**

European Conferences:

- **DATE** IEEE Design Automation and Test in Europe Conference
- **EuroSys** The European Conference on Computer Systems
- **EURASIP** European Conference on Speech and Image Processing, Multimedia Communications and Services
- **Euro-Par** Parallel and Distributed Architecture Conference

Journals:

- IEEE Transaction on Computers
- IEEE Transactions on Parallel and Distributed Systems
- Journal of Parallel and Distributed Computing
- IEEE Design & Test Magazine
- IEEE Micro
- ACM Transactions on Architecture and Code Optimization
- Transactions on Reconfigurable Technology and Systems (TRETs)

- JSA Journal of Systems Architecture (Elsevier)
- Pervasive and Mobile Computing (Elsevier)

To ensure the quality of publications, and protect the IPR (Intellectual Property) generated within the project, the consortium has decided during the ExaNoDe kick-off meeting that the intention of publication of a scientific paper should be notified to the whole consortium at least 45 days before the submission deadline. The leading partner, or partners in case of joint publication, will provide a brief description of the publication, to allow the rest of the consortium to verify the content of the publication.

4.2 Open-access to publications

The ExaNoDe consortium has decided to take a case-by-case approach related to open access publications. Once a publication has been approved by the whole consortium, to avoid any IP or confidentiality breach, and an editor has been identified, all the authors (or co-authors in case of multi-partner publications) might decide to provide open-access to the paper. Such papers will be stored in an open-access repository connected to the tools proposed by the European commission (e.g. open AIRE).

A Data Management Plan (DMP) will describe in detail how open publications are handled. The DMP for the Pilot on Open Research Data will be defined and delivered. This will result in a deliverable D1.0 due at M6.

5 Contribution to standards

During the life-cycle of the ExaNoDe project various software components, part of OpenSource standards will be enhanced to benefit for the project outcomes. In particular the consortium has identified as the set of standard to which the ExaNoDe project will contribute.

Linux Kernel and KVM extension: Patches will be made available and notified to appropriate gatekeepers

ARM Generic Trusted Firmware: Changes and/or finding will be made known to the community developing this firmware through their specific new group.

UEFI (Unified Extensible Firmware Interface) system boot and initialization: Through postings of changes and patches to the technical discussion forum

MPI forum, OpenStream, OpenMP and GASPI: enhancements will be presented to the standardisation forums. If accepted they become part of the standard in question and thus part of all future implementations.

All the contributions to standards, besides the code patches, will be released on a dedicated section of the ExaNoDe project website.

6 Organization of a workshop

Workshops are renowned to be a really effective dissemination venue where scientists from a specific field, or a field related to the topic of the workshop can gather to present their work and receive feedback from the other participants. Workshops are also usually attended by industry members looking for new ideas/technologies to improve their future products.

During the course of the project the consortium will identify a target to host an ExaNoDe workshop, being it either a special track on HPC (High Performance Computing) Core Technologies of an international conference, or a workshop dedicated to the project.

A dedicated deliverable (D6.5) at M36 will provide the details of the workshop organized for the ExaNoDe project.

7 Dissemination of software and applications

European industries and academy will surely benefit from the adoption of the software and applications developed during the execution of the project. To facilitate the access to such software a public repository will be created where (when applicable) software components developed by the partners of the project will be stored to be accessible by a public audience. To enforce this type of releases, a notice on the website of the project, or also of the beneficiary partner, shall be published in order to widen the necessary visibility.

A Data Management Plan (DMP) will describe in detail to collect, organize, back-up, and store the data that will be generated throughout the project. The DMP for the Pilot on Open Research Data will be defined and delivered in Task 1.2, with a dedicated deliverable D1.0 due at M6.

Besides releases confined to the boundaries of the project, another important channel for software dissemination is the OpenSource community. During the execution of the ExaNoDe project various well-known software frameworks (e.g. MPI libraries, OpenMP programming model) and operating systems (e.g. Linux) will be extended to leverage the novelties introduced by the ExaNoDe project. Such extensions should be submitted to the relevant communities and standardization bodies (such as the OpenMP language committee) in order to obtain early feedbacks and an easier adoption process in the future.

8 Dissemination actions

The ExaNoDe consortium has identified a set of stakeholders, which correspond to the project's potential target groups, each of them requiring a set of tailored dissemination actions:

1. General public
2. Public authorities and policy makers
3. Application sectors/industries
4. Engineers and Scientists

In the table below dissemination activities are summarized for each different target stakeholder group, together with a metric to evaluate the level of dissemination.

Table 1: Dissemination actions

Stakeholder identification	Actions	Responsibility	Realization	Metrics
Scientific community	Submit papers	All participants	Submission to conferences, contributions to fairs	Number of accepted papers per fair
Scientific community	Submit papers	Academic participants	Submissions to journals	Number of submission or cited project publications
Students	Organize courses, PhD theses	Academic participants	Provide course materials, host PhD Theses	Number of courses, theses
Industrials	Provide information on project results - focus on industrial aspects	All participants	Attending industrial conferences, set up of booths. Create and develop industrial advisory board.	Number of booths, contracts
Public Community	Provide information on project results - focus on societal aspects and applications	Dissemination WP leader, all participants	Newsletter, public website, video, etc.	Number of newsletter subscription, or visits of public website
European Commission	Provide information on results - focus on impacts	Project coordinator	Deliverables, submission to EC journals	Evaluation from the EC, number of journals
Other HPC projects (ExaNeSt, EcoScale, Euroserver)	Provide information on strategy and results from ExaNoDe. Coordinate inter-project dependencies (prototype deliveries)	All participants, dissemination and WP leaders	Organizing common meetings	Number of common meetings
ETP4HPC	Provide information on project results and feedback on SRA.	ExaNoDe partners members of ETP4HPC	Participating to ETP4HPC events	Reuse of ExaNoDe results by ETP4HPC
Other EU Projects or national activities	Provide information on project results	Coordinator and all participants	Public website, project or public events	Number of meetings, interest of other projects

9 Dissemination groups

The goal of the ExaNoDe project is to build the core components for the next generation computing node that can be used for the definition of next-generation Exa-Scale machines. The scientific work performed in the project will introduce novelties in different areas spanning from silicon interposer technology, memory technology, to system software and resources virtualization. Each of these groups has a clear and different target audience (stakeholders), as reflected in the dedicated dissemination plan.

9.1 Silicon interposer design and manufacturing

The technology developed inside the ExaNoDe project can be presented to different types of conference:

- scientific
- integration & packaging
- product & market

First, the complete realization of a large interposer with top dices stacked, and its packaging, constitute a relatively advanced and innovative work. The full integration, associated with some electrical data may be of high interest at scientific device conference. **IEDM** (International Electron Devices Meeting) is the bigger and very selective conference to which ExaNoDe partners could apply.

The 3D and packaging technologies that are proposed to be used for the interposer and the chiplet are more often than not introduced in IEEE conferences such as **3DIC** (International 3D Systems Integration Conference) or **ECTC** (Electronic Components and Technology Conference). Those are the major conferences which gather worldwide experts in 3D a packaging. Some **Imaps** conferences, such as the annual International Symposium of Microelectronics, suit also very well with the scope of ExaNoDe work.

Furthermore, from the market point of view, we can cite 2 workshops dedicated to 3D technologies: one in US, **ASIP 3D** (Architectures for Semiconductor Integration and Packaging Symposium) - the other one is Semi workshop “**TSV conference**”, in Europe. Those workshops offer, on invitation, the possibility to introduce advanced work in 3D and packaging.

CEA-Leti is present on different stand (regular presence at ECTC – TSV Summit – Imaps, etc.). The ExaNoDe poster can be exposed in such events to publicize the developed technology and project objectives.

Concerning a paper in a journal, some of the above conferences propose a publication in a journal. Additionally, **Chip Scale Packaging** for instance is a worldwide journal, well known from industrial, and in which integration could be detailed.

9.2 Memory Technology

ExaNoDe will analyse suitability of high-end and next-generation memory solutions for HPC. For the ExaNoDe architecture itself, attention is focused on the DRAM solutions: DDR4 with in-memory ECC, LPDDR4, LPDDR4 with in-memory ECC, Hybrid Memory Cube and High Bandwidth Memory. In the last phase of the project, various NVMs (Non-Volatile memories) will also be studied, to build heterogeneous systems that combine various technologies (e.g.

DRAM and NVMs). The outcomes of this analysis will be summarized in scientific publications.

The list of the most relevant target conferences and journals for the presentation of ExaNoDe's achievements is:

Conferences

- **MEMSYS**, The International Symposium on Memory Systems
- **SC**, IEEE Supercomputing Conference
- **ISC**, International Supercomputing Conference
- **ISCA**, IEEE International Symposium of Computer Architecture
- **MICRO**, IEEE/ACM International Symposium on Microarchitecture
- **SAMOS**, International Symposium on Systems Architectures Modeling and Simulation
- **PACT**, Parallel Architectures and Compilation Techniques
- **IPDPS**, IEEE International Parallel & Distributed Processing Symposium
- **HPCA**, IEEE International Symposium on High-Performance Computer Architecture
- **HPPC**, IEEE - High Performance Computing and Communications

Journals

- **TC**, IEEE Transaction on Computers
- **TPDS**, IEEE Transactions on Parallel and Distributed Systems
- **JPDC**, Journal of Parallel and Distributed Computing
- **IEEE Micro**
- **TACO**, ACM Transactions on Architecture and Code Optimization

9.3 System Software

The system software development task in ExaNoDe will provide the necessary firmware and operating system support for the project's prototypes, including support for shared, virtualized high-speed peripherals (e.g. RDMA engines and Ethernet NICs), switching/routing, dynamic memory management compatible with the UNIMEM memory architecture, and efficient interaction with accelerators.

The development of system software for the ExaNoDe prototypes will provide opportunities for scientific publications. The most relevant conferences and journals, to be targeted, include the following:

Conferences:

- **USENIX ATC** (Annual Technical Conference)
- **ACM ASPLOS** (Architectural Support for Programming Languages and Operating Systems)
- **HPCA**, IEEE International Symposium on High-Performance Computer Architecture
- **HiPEAC** Int. Conference on High Performance and Embedded Architectures and Compilation
- **ACM SYSTOR** Systems & Storage Conference
- **ACM ICS** International Conference on Supercomputing

Journals:

- **JPDC**, Journal of Parallel and Distributed Computing

- **TACO**, ACM Transactions on Architecture and Code Optimization
- **Journal of Systems and Software**

Moreover, we see the potential for feedback into university-level education, as our technologies mature during the project timeline, by encouraging future researchers to pick their research topic from activities inherent to the ExaNoDe project. In addition, to attract university students, there will be the possibility to work hands-on on topics related to the project.

A further dissemination measure will be the participation in exhibitions and tradeshow aimed at presenting the project results to industrial managers and specialists from relevant sectors. This line of dissemination will also consider ICT Theme Events run by the European Commission.

9.4 Parallel Programming Models and runtimes

ExaNoDe will study how the UNIMEM architecture can potentially benefit programming models and runtime libraries for HPC. The novel UNIMEM architecture principle of “access anything from everywhere” can significantly affect the programming models, both from the perspective of performance and coding productivity. The mix of partners involved and their expertise will allow broad coverage of various flavours of parallel programming models, including shared memory (OpenMP, OmpSs, OpenStream), message passing (MPI) and PGAS (GPI) parallel programming paradigms. Research throughout ExaNoDe should extend these well-known programming models and contribute to the respective communities by providing novel advanced features. Moreover, the work in ExaNoDe should provide new insights to steer programming models standardization bodies (such as the OpenMP language committee).

Also, due to strict power consumption constraints of exascale, ExaNoDe will dedicate to exploring runtime libraries for power and thermal management.

The exploration of parallel programming model and runtime libraries should result in scientific publication. The publications should target major conferences and journals, such as:

Conferences:

- **SC** IEEE Supercomputing Conference
- **ISC**, International Supercomputing Conference
- **ICS**, ACM International Conference on Supercomputing
- **DAC** IEEE Design Automation Conference
- **ISCA** IEEE International Symposium of Computer Architecture
- **MICRO** IEEE/ACM International Symposium on Microarchitecture
- **HiPEAC** Int. Conference on High Performance and Embedded Architectures and Compilation
- **PPoPP**, ACM SIGPLAN symposium on Principles and practice of parallel programming
- **PACT**, Parallel Architectures and Compilation Techniques
- **PLDI**, ACM SIGPLAN symposium on Programming Language Design and Implementation
- **PACT**, Parallel Architectures and Compilation Techniques
- **IPDPS**, IEEE International Parallel & Distributed Processing Symposium
- **HPCA**, IEEE International Symposium on High-Performance Computer Architecture
- **CLUSTER**, IEEE - Cluster Computing and Workshops

- **DATE** IEEE Design Automation and Test in Europe Conference
- **Euro-Par** Conference

Journals:

- **IEEE Micro**
- **TPDS**, IEEE Transactions on Parallel and Distributed Systems
- **JPDC**, Journal of Parallel and Distributed Computing
- **TACO**, ACM Transactions on Architecture and Code Optimization

9.5 Virtualization of system and resources

ExaNoDe will study virtualization in the field of HPC. The combination of virtualization techniques with the architectural novelties introduced in the ExaNoDe project (e.g., high performance memory technologies, the UNIMEM memory model) will create the disruption needed to make virtualization suitable for the HPC domain. Virtualization will in fact provide a twofold benefit to the project, and HPC systems in general:

- it will provide acceleration to the application level via the parallel programming model studied in the project, by virtualizing the accelerators.
- It will increase the efficiency and reliability of the system by providing migration and snapshotting capabilities.

The virtualization Hypervisor used in the project is QEMU/KVM (an Open Source Hypervisor based on Linux). The novelties introduced in the project will be of primary importance to increase the domains targeted with KVM, by adding HPC systems to the paramount of possible targets. A continuous dissemination towards the OpenSource community is the key to maximize the possibility for the project outcomes to become available in upstream versions of the Hypervisor source code, and thus available on production machines. Dissemination at this level will take place by submitting code patches to the relevant mailing lists: *kvmarm* and *qemu-devel*.

Besides OpenSource contributions, novelties and improvements in virtualization techniques will be disseminated through scientific papers to the major European conferences either specific for the virtualization field, or dedicated to HPC in order to increase the interest in virtualization.

Conferences are:

- **ACM ASPLOS** (Architectural Support for Programming Languages and Operating Systems)
- **ISC**, International Supercomputing Conference
- **ICS**, ACM International Conference on Supercomputing
- **HiPEAC** Int. Conference on High Performance and Embedded Architectures and Compilation
- **DATE** IEEE Design Automation and Test in Europe Conference
- **IPDPS**, IEEE International Parallel & Distributed Processing Symposium


10 Concluding Remarks

This deliverable presents the plan for the dissemination of the ExaNoDe project outcomes. The plan is divided in several activities, identified as the key to ensure a fruitful dissemination of the project outcomes to the public audience, research and industry community.


The ExaNoDe consortium will consider dissemination activities as important as the technical work carried on in each task, to maximize the impact of the project and get feedback from outside the project environment to drive the work performed in a successful manner.

11 ANNEX A: Poster presented at Supercomputing 2015 (Emerging Technologies Exhibits)

A first project poster has been submitted and accepted for Emerging Technologies Exhibits during Supercomputing conference in Austin. It is represented below:




Future and Emerging Technologies (FET)
TOWARDS EXASCALE HIGH PERFORMANCE COMPUTING




ExaNoDe


EUROPEAN EXASCALE PROCESSOR MEMORY NODE DESIGN




Coordinator




Fraunhofer




European Supercomputing Center



KALRAY



Centre National de la Recherche Scientifique




Virtual Open Systems

Contact : denis.duboh@cea.fr

ExaNoDe

ExaNoDe Investigates, develops and pilots:

- a highly efficient,
- highly integrated,
- high-performance,
- heterogeneous compute element aimed towards exascale computing.



Mid-applications
Workstation
Parallel programming
OS, Firmware

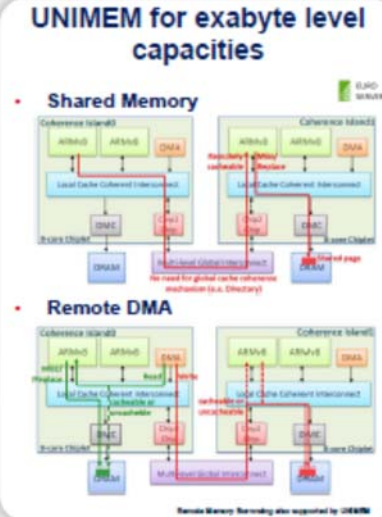
Compute Node

Compute Unit

Multisite project general information	
Project title	European Exascale Processor Memory Node Design
Starting date	October 1st, 2015
Duration	36 months
Call number	101016-1-IP1WPC-2014
Topic	IP1WPC-1-2014 HPC Core Technologies, Programming the hardware and Algorithms for Extreme Parallel and System Scale Applications
Keywords	Energy Efficiency, HPC, Low Power, Processor, Memory Architecture, 3D integration, CoE, Burden, MPI, Workstation, Mid-applications
Budget	815M

UNIMEM for exabyte level capacities

- Shared Memory**
- Remote DMA**



Remote Memory Forwarding also supported by UNIMEM

ARM-v8 processors for energy efficiency

ARM® Cortex™-A72: Highest Performance ARM Cortex Processor

Scalable performance from mobile to high performance computing


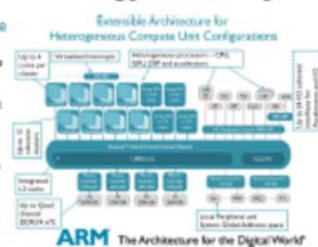
- Platform retained device performance
- 75% less energy for same workload scaling denser and cooler devices

Competing scalable solutions

- From single CPU to 48-way full SMP
- Non-FP FCP enables high frequency designs

Designed with the system in mind

- Comedia GCS 580 microcontroller
- Hi4-T88 GPU V553 Video DP530 Display
- PMU488, FIC-408, EA-300


ARM The Architecture for the Digital World

ExaNoDe as part of a global strategy


EURO SERVER

Redesigns the enterprise server:


- Lower cost through system integration
- Energy efficiency: maximum use of processor and reuse of server resources
- Scalability of I/O resources



Focuses on acceleration







European Exascale System Interconnect and Storage - www.esasnet.eu




3D interposer integration for compute density


- Challenges**
- Proposal**



This ExaNoDe research project is supported by the European Commission under the "Horizon 2020 Framework Programme" with grant number 671570



12 Glossary

ACM	Association for scientific and educational computing
DDR4	Fourth generation of synchronous dynamic random-access memory
ETP4HPC	Framework for stakeholders, led by industry, to define research priorities and action plans on High Performance Computing
GASPI	Project to define a novel specification for an API based on GPI
IEEE	Foundation for educational and technical advancement of electrical and electronic engineering, telecommunications, computer engineering and allied disciplines
LPDDR4	Low-Power DDR4 memory
MPI	Standardized and portable message-passing system designed for parallel computers
OpenMP	API for multi-platform shared-memory parallel programming in C/C++ and Fortran
OpenStream	Stream programming language, designed as an incremental extension to the OpenMP parallel programming language, and allowing to express arbitrary dependence patterns between tasks in the form of task-level data flow dependences
PGAS	Global memory address space that is logically partitioned and a portion of it is local to each process or thread
QEMU/KVM	Open Source virtualization hypervisor based on Linux
SIGPLAN	Association for Computing Machinery's Special Interest Group on programming languages
UEFI	Standard firmware interface for personal computers, designed to replace BIOS (basic input/output system)
UNIMEM	Memory abstraction for distributed systems to enable actual memory sharing between different computing islands (nodes)
USENIX	Advanced Computing Systems Association, focusing primarily on the study and development of Unix and similar systems
TSV	Vertical electrical connection (via) passing completely through a silicon wafer or die