



D6.1

Project External Website, project flyer and social media presence

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Executive Summary

Among the primary goals of the European Commission funding schemes, aiming at ensuring the European strategic position on target technical fields, there is a need to maximize the impact of projects. The project's dissemination activity is designed to address various societal, economical and scientific challenges. In addition, the dissemination activity is considered as the vehicle for innovation. One of its aims is to develop a publicly visible outcome for the scientific community with flyers, website, and social media presence.

As part of the dissemination activities for public stakeholders, this document presents the currently available version of the ExaNoDe project web-presence.

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1 Introduction

In the digital era it is of extreme importance to have a well-designed presence on the web, to maximize the size of the audience which can be reached, and the information which can be shared. Seamlessly, this is true for a research project as the second major factor of success is the creation of awareness and the pervasive dissemination of the results.

The ExaNoDe project is present on the web by means of a dedicated domain which is used to provide a website, providing to public users general information about the project goals and ambitions, the partners involved, the list of the publications, and a main contact to be used in case further information are needed. Such a website takes into account continuous content publication with the intent of maximizing the visibility through search engines.

In addition to the website, dedicated social media (e.g., Twitter, LinkedIn) accounts for the ExaNoDe project will be created, to further improve the amount of information spread across the web.

To enforce the identity of the project a logo univocally identifying the project and a flyer has been designed in order to be used, the former as identification mark in every formal/informal document, the latter in conferences or other venues where the project participates.

2 Project identity

The main aim of identity is to make the public aware of the ExaNoDe project. Public stakeholders are the scientific community and industrial entities. At the beginning of the project a logo, a domain name and a website have been created. The logo univocally identifies the project. The website is designed, as the basic infrastructure for publicizing the project. In addition a poster, a technical brochure and flyers describing the goals of the project have been prepared, to be used during international events (as shown in Section 2.3). The vehicles to create awareness for the project will be maintained and updated throughout the duration of the project, ensuring a knowledgeable and continual presentation of ExaNoDe at relevant events.

2.1. *ExaNoDe Visual Design and style-guide*

A key item within the project identity is the project logo which is presented below.



Figure 1: Project logo

While the blue colour and yellow stars suggest Europe, the logo highlights the main objectives of the project through a clear view of the word “Exa” for exascale and the word “NoDe” for compute node. The broken line underneath “NoDe” reflects both interposer integration and scalability.

2.2. External web site and social media

The ExaNoDe project is present on the web by means of a website: <http://www.exanode.eu>, providing to public users general information about the project goals and ambitions, the partners involved, the list of the publications, and a main contact to be used in case further information are needed. It details the project concepts, vision, objectives and expected outcomes as well as public documents, deriving from the project work. These will be regularly updated, offering links to other relevant sites and links to partners' websites.



Figure 2: ExaNoDe web site front page

ExaNoDe plans to establish a presence on well-known social networking sites (LinkedIn, Twitter). The social network presence will be regularly updated.

2.3. *Dissemination Pack*

2.3.1. Project flyer

An initial flyer has been designed and distributed during the SC15 conference and exhibition (as described in 2.3.2). That flyer will be mapped into the revised project style guide and made available on the website at the beginning of the 2nd project quarter. It provides information about the project, its objectives and future achievements.

2.3.2. Generic poster, brochure and presentation

A generic poster has been initially designed for the SC15 conference for “Emerging Technologies Exhibits”. ExaNoDe was selected as one of the research exhibits in the “Emerging Technologies” Technical Program track of the SC15 conference that took place in Austin, Texas (<http://sc15.supercomputing.org/program/emerging-technologies>).

The Emerging Technologies track showcased innovative technologies considered to have the potential to significantly change and extend the world of HPC in the next five to fifteen years. A particular focal point was emerging System-on-a-Chip (SoC) technologies for HPC. ExaNode presented an overview of the project, the technology targets and an overview of the ongoing architectural design development.

The SC15 poster is represented below:



Future and Emerging Technologies (FET) TOWARDS EXASCALE HIGH PERFORMANCE COMPUTING



ExaNoDe EUROPEAN EXASCALE PROCESSOR MEMORY NODE DESIGN



ExaNoDe

ExaNoDe investigates, develops and pilots:

- a highly efficient,
- highly integrated,
- high-performance,
- heterogeneous compute element aimed towards exascale computing.

ExaNoDe project general information

Project title	European Exascale Processor Memory Node Design
Starting date	October 1st, 2015
Duration	36 months
Call identifier	H2020-FET-PC-2014
Topic	FET-PC-2014 HPC Core Technologies, Programming Environments and Algorithms for Extreme Parallelism and Extreme Data Applications
Keywords	Energy Efficiency, HPC, Low Power Processors, Memory, Accelerators, 3D-integration, OS, Runtime, MPI, Virtualization, Mini-applications
Budget	8.6 M€

Compute Node

Compute Unit

ExaNoDe prototype

WP1: Management
WP2: Co-Design for Exascale HPC systems
WP3: Enablement of Software Compute Nodes
WP4: Compute node design and validation
WP5: System Integration & Evaluation
WP6: Dissemination and Exploitation
Project Implementation

UNIMEM for exabyte level capacities

Shared Memory

Remote DMA

Remote Memory Borrowing also supported by UNIMEM

ARM-v8 processors for energy efficiency

ARM® Cortex™-A72: Highest Performance ARM Cortex Processor

Extensible Architecture for Heterogeneous Compute Unit Configurations

Scalable performance from mobile to high performance computing

- Maximizes sustained device performance
- 75% less energy for same workloads enabling slimmer and cooler devices

Compelling scalable solutions

- From single CPU to 48-way full SMP
- 16nm FF POP enables high frequency designs

Designed with the system in mind

- CoreLink CCI-500 interconnect
- Mali-T880 GPU, V550 Video, DP550 Display
- MMU-400, NIC-400, ELA-500

ARM The Architecture for the Digital World™

ExaNoDe as part of a global strategy

EURO SERVER

redesigns the enterprise server:

- Lower cost through system integration
- Energy efficiency - low-power 64 bit processor and more efficient software
- Multitasking of I/O resources

focuses on acceleration

European Exascale System Interconnect and Storage - www.exanet.eu

Storage fast, distributed in-node non-volatile memory

Interconnect low-latency, unified compute & storage traffic

Packaging advanced, liquid-cooled

App's real, scientific and datacenter

Prototype 1000+ ARM cores from EuroServer ARM nodes with UNIMEM address space & shared I/O from ExaNoDe Chiplets, Si Interposer with ECOSCALE Hetero ARM+FPGA's

Scalable Liquid Fully Increased Cooling Technology

3D interposer integration for compute density

Challenges

- High density of connection between chiplet and interposer
- thermal management
- Large (typically more than 300mm²) and thin (typically less than 200µm) silicon interposer ⇒ thermo-mechanical issue

Proposal

- Maximize Si thickness to ease warp management
- Propose a density of interconnection compliant to system specification
- Minimize inter die gap
- Propose a scheme of manufacturing to ease packaging (chiplet on interposer on BGA)
- Propose thermal solution for spreading (thermal polymer - Lid etc...)

Background

2012: Womring: WideIO-on-logic stack

2015: 3D-NOC: logic-on-logic stack



This ExaNoDe research project is supported by the European Commission under the "Horizon 2020 Framework Programme" with grant number 671578



Figure 3: ExaNoDe generic poster

In addition, a two page brochure reinforces this poster with technical details.

ExaNoDe: European Exascale Processor & Memory Node Design

Abstract - ExaNoDe is a collaborative European project within the "Horizon 2020 Framework Programme", that investigates and develop a highly integrated, high-performance, heterogeneous System-on-a-Chip (SoC) aimed towards exascale computing. It is addressing these important challenges through the coordinated application of several innovative solutions recently deployed in HPC: ARM-v8 low-power processors for energy efficiency, 3D interposer integration for compute density and an advanced memory scheme for exabyte level capacities. The ExaNoDe SoC will embed multiple silicon "chiplets", stacked on an active silicon interposer in order to build an innovative 3D-Integrated-Circuit (3D-IC). A full software stack allowing for multi-node capability will be developed within the project. The project will deliver a reference hardware that will enable the deployment of multiple 3D-IC System-on-Chips and the evaluation, tuning and analysis of HPC mini-apps along with the associated software stack.

The main objective of the ExaNoDe project is to deliver a compute device that will meet the scaling and performance requirements for exascale computing. The compute device will be for pilot-level use by system integrators, software teams and subsequent evaluation through industrial deployment. ExaNoDe is a European collaborative project with a total budget of €8.6M, fully contributed by the European Commission within the Horizon 2020 Framework Programme (H2020). The project starts in October 2015, and will run for three years. The ExaNoDe consortium, coordinated by CEA, has thirteen partners, who bring complementary expertise across the entire HPC research and development value chain (CEA, ARM, Atos, VOSYS, KALRAY, Scapops, BSC, Fraunhofer, Juelich, CNRS, FORTH, ETH Zürich and University of Manchester).

The ExaNoDe system architecture is based on the coordinated application of several key recent innovations: ARMv8 Cortex 64-bit processors, 3D interposer integration technology and an advanced memory scheme for exabyte capacities.

Over the last few years, there has been a growing interest in using the 64-bit ARM cores outside the mobile and embedded sectors, in data centers^{1,2} and for high performance computing³. ExaNoDe builds on these previous projects, which have done much of the important groundwork in demonstrating the feasibility of the modern ARM-v8 cores for HPC and improving the maturity of the ARM software stack.

ExaNoDe will also take advantage of 3D packaging via the use of active silicon interposer integration. As illustrated in the adjacent figure, multiple dies ("chiplets"),

¹Energy-conscious 3D Server-on-Chip for Green Cloud ("EuroCloud"), EU FP7 project 247779, <http://www.eurocloudserver.com>.

²EUROSERVER, Green Computing Node for European micro-servers, EU FP7 project 610456, <http://www.euroserver-project.eu/>

³Mont Blanc, European scalable and power efficient HPC platform based on low-power embedded technology, EU FP7 project 288777, <http://www.montblanc-project.eu/>

ExaNoDe – SC15 Emerging Technologies

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for example compute chiplets, are stacked side-by-side in a face-to-face configuration on an active silicon interposer. This 3D packaging approach for System-on-a-Chip increases compute density by integrating multiple chiplets, improves manufacturing yield by using smaller dies, reduces core-to-core and core-to-memory distances, and greatly reduces the cost of hardware customization with dedicated logic in the active interposer. In addition, it is planned within the ExaNoDe project to add another level of integration with a Multi-Chip-Module embedding several 3D-Integrated-Circuits (3D-IC) with FPGA and DRAM bare dies to build the complete ExaNoDe compute device.

With today's programming models (such as the Partitioned Global Address Space - PGAS), the hardware needs to move and duplicate data between different non-contiguous memory spaces using techniques such as Remote Direct Memory Access, RDMA. The capabilities of the ExaNoDe hardware system architecture will provide a true global address space (GAS), without the need for managed abstractions to move data between partitions. This global shared address space leverages the capabilities of the modern ARMv8 processor to create a global shared memory up to 256TByte in size. A full software stack allowing for scalable and multi-way heterogeneous capabilities will be developed within the project.

The ExaNoDe project will develop a prototype with successive phases. Early in the project, the multi-board prototype will be used to develop the SW framework. Then, the 3D-IC compute device will be manufactured and integrated with FPGA and memory units in a module. The final phase will be the ExaNoDe system-level prototype that will integrate together the SW framework, the mini-applications, and the ExaNoDe 3D-IC. This prototype will measure the performance of the mini-applications as well as their energy/power consumption.

With ExaNoDe project, we argue that 64-bit ARM cores combined with 3D integration and Global Address Space will bring a dramatic change in HPC architecture for lower system cost and higher energy-efficiency.

Acknowledgement:

This research project is supported by the European Commission under the H2020 Framework Programme under the "HPC core technologies and architectures" topic, with grant number 671578.

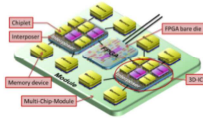


Figure 4: ExaNoDe technical brochure

Finally, a generic and public presentation has been developed to provide each partner with dissemination materials.

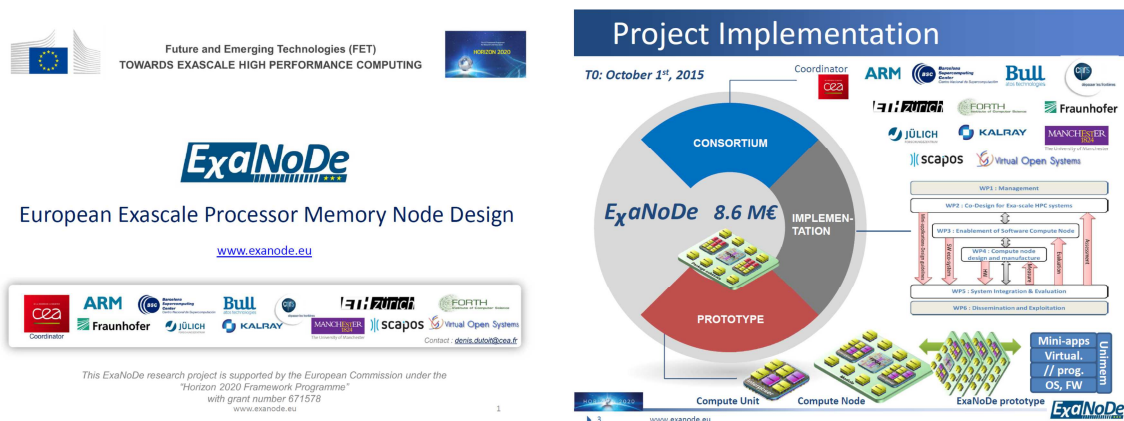


Figure 5: Extract of ExaNoDe presentation

All dissemination pack is available from the project repository so that all partners could share the same project identity with their local scientific community and industrial entities. It is also available from the project website for public stakeholders.

3 Concluding Remarks

This deliverable presents the public materials for the dissemination of the ExaNoDe project outcomes. The dissemination strategy is divided in several media, identified as the key to ensure a fruitful dissemination of the project outcomes to the public audience, research and industry community.

The ExaNoDe consortium will consider public dissemination activities as important as the technical work carried on in each task, to maximize the impact of the project and get feedback from outside the project environment to drive the work performed in a successful manner.